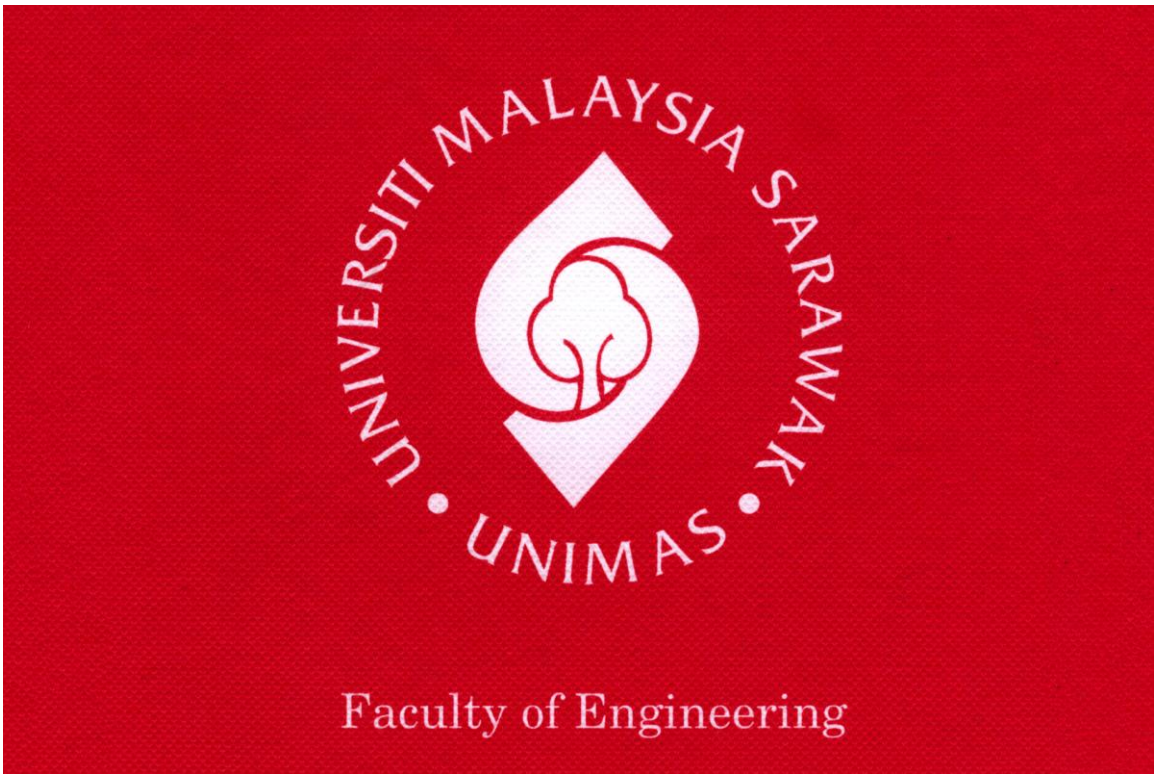

POWER AMPLIFIER FOR SOFTWARE DEFINED RADIO

Dahlan Bin Samat

Bachelor of Engineering with Honors
(Electronic & Telecommunication Engineering)
2009

UNIVERSITI MALAYSIA SARAWAK

R13a

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Judul: **POWER AMPLIFIER FOR SOFTWARE DEFINED RADIO**

SESI PENGAJIAN: 2008/2009

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POWER AMPLIFIER FOR SOFTWARE DEFINED RADIO

DAHLAN BIN SAMAT

This project is submitted in partial fulfilment of
The requirements for the degree of Bachelor of Engineering with Honours
(Electronics and Telecommunication Engineering)

Faculty of Engineering
UNIVERSITI MALAYSIA SARAWAK
2008/2009

This Final Year Project attached here:

Title : Power Amplifier for Software Defined Radio

Student Name : Dahlan Bin Samat

Matric No : 13924

has been read and approved by:

_____ _____

Mdm. Rohana Binti Sapawi Date

(Supervisor)

Dedicated to beloved family

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ABSTRAK

Projek ini mengkaji ciri-ciri tiga jenis litar “Power Amplifier (PA)” yang akan di aplikasikan untuk “Software Defined Radio (SDR)”. Ketiga-tiga litar tersebut adalah “Conventional PA”, PA dengan transistor NPN dan PA dengan transistor NMOS. Selain itu, teknik tambahan turut diaplikasikan ke dalam setiap litar untuk menambah tahap kecekapan litar-litar tersebut. Simulasi akan dilakukan terhadap litar menggunakan program simulasi PSpice versi 9.2. Analisa dijalankan dengan memanipulasikan frekuensi-frekuensi yang digunakan untuk “Global System for Mobile Communication (GSM)”. Perbandingan akan dibuat berdasarkan keupayaan litar yang dikaji dari segi penggandaan, dan keupayaan menggandakan kuasa sumber dari input. Keputusan simulasi menunjukkan litar “PA” yang menggunakan transistor NMOS mempunyai keupayan dan tahap penggandaan input kepada jumlah yang sepatutnya. Dengan tambahan teknik melaui litar “Doherty amplifier” juga telah menambah baik keupayaan litar tersebut.

ABSTRACT

This project investigates the characteristics of three types of Power Amplifier (PA) circuit that will use in the Software Defined Radio (SDR). The circuits are Conventional PA, the proposed PA using NPN transistor, and the proposed PA using NMOS transistor. In addition, the circuit will be constructing with efficiency-boosting technique circuit that is using Doherty Amplifier. The simulation of the circuit will be done by using the PSpice version 9.2 simulation software. The analysis will be done by manipulating the operating frequency that is suitable for Global System for Mobile Communication (GSM) application. The comparison that will be analyzed is the efficiency of the circuit and the output gain. The outcome of the results shows that the PA circuit using the NMOS transistor give high efficiency and gain. With the addition of the Doherty amplifier also has increased the performance of the circuit.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 Introduction

As the 3G and 4G are introduced, the evolution of wireless communication standards is much accelerated by this the existing multi-standard transceiver should be improved to give the transceiver become much more inconvenience with the smooth migration to future generation wireless standards, convergence of wireless services, and international roaming.

Power amplifier (PA) is one of the most difficult components for multi-standard radio frequency (RF) transceiver. The multi-standard PA that implemented must be satisfied the wide range of requirement such as frequency band, dynamic range, and bandwidth. It also means the PA design must appropriate to the requirement of the several applications that will be performing by software defined radio (SDR). The several applications are refer to 3G, Bluetooth, local area 802.11 networks, Code Division Multiple Access (CDMA), Global System for Mobile Communication (GSM)

and others wireless application. Therefore, the multi-standard PA should be comparable with a single standard PA in size, power consumption, efficiency, linearity, gain and also the noise figure (NF) that related to the performances of PA.

In the electronic production industry, the main issues about PA designing are related to the efficiency and the linearity of PA. Both of these parameters will affect the performances of PA to amplify the continuous output of information signal. With the efficiency of PA is determined by taking a ratio of RF output power to direct current (DC) input. This parameter becomes dominant in the PA designing because the entire designer wants to have an ideal design that will produce 100% efficiency amplification. Even though the ideal PA will not easily to achieve this day, but there are several solutions that have been produce to achieve higher efficiency. Thus, several classes of PA has been created to give the power efficiency can be increased up 100%. Even though the power efficiency of one of the PA class is stated to be perfect (refer to class C), but this condition only exists for the ideal PA operation when assuming there is no power consumption occurs. Beside the various classes created, the technique used is the Doherty amplifier. It was build by using multiple amplifiers, with each of it responsible for amplification over some subset of the overall power range [1].

Besides that, the other main parameter is linearity. This characteristic is important to have low distortion and high power efficiency for PA. This parameter can be minimized by the techniques that will improve the linearity and facilitate operation with less back off and high frequency [2]. The techniques used to improved linearity such as Cartesian feedback, feed-forward, and etc. Other issue that will be influence PA performance will be about gain, and noise figure (NF).

In this project, Doherty Amplifier circuit will be used as an approaching to achieve the highly power efficient for non-linear class C PA. Thus, the linearity will be improving more as much as it can. The linearization techniques that will be discussed in this project will be Cartesian feedback. Therefore, the comparable of the efficiency between the theoretically and the simulation result will be defined.

1.2 Project Objectives

1.2.1 Investigate the roles of reconfigurable of power amplifier in software define radio.

1.2.2 Design and restructure the architecture of PA for software defined radio's RF antenna transceiver.

1.2.3 Compare the result between the conventional PA and proposed PA class C.

1.3 Chapter Outline

This report is divided into 5 chapters and each chapter organized as follows;

Chapter 1 explains the aims and the objectives of the project that will be carried out. This chapter also provides the problem statement of the reconfigurable of PA for SDR.

Chapter 2 is literature review, which will discuss the definition, the structure, and the application of SDR. The classes and the characteristic of each classes of PA are also will be discussed. Beside that this chapter will review the related journal that present the issues about the efficiency, linearization of the PA design and the technique used to improve these two metrics.

Chapter 3 is about the methodology that will be used to design a good performance of the PA section that will meet the requirement for the SDR. This chapter also will discuss about the PA design from the proposed and conventional class C with these circuit will be integrated with the linearization and efficiency-boosting techniques. Then, the circuit design will be simulated using P-Spice software that will guide the whole designing and simulation process.

Chapter 4 discusses the results that have been achieved by proposed class C PA and conventional class C design. The results from the simulation will be compared with the theoretical specification of the class of amplifier used. The comparable is due to the performance, the frequency uses, the power consumption, and the efficiency.

Chapter 5 is the conclusion of the overall project report that successfully carried out. In addition, the recommendation for further work that can be implemented to improve this project also is being discussed.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction to SDR

With the increase of wireless standards as well as wide area 3G, 2.5G, and local area 802.11 networks, future wireless devices will need to support multiple air-interfaces and modulation formats [3]. SDR technology enables such functionality in wireless devices by using a reconfigurable hardware platform across multiple standards.

Recently, SDR has been suggested as the solution to meet the variety of requirements. Some of the advantages that provide by SDR to the customer are in form of information appliance, which is always connected, despite the location, communicating voice and data. SDR bring the ability to access the various form of communication through a compact transceiver.

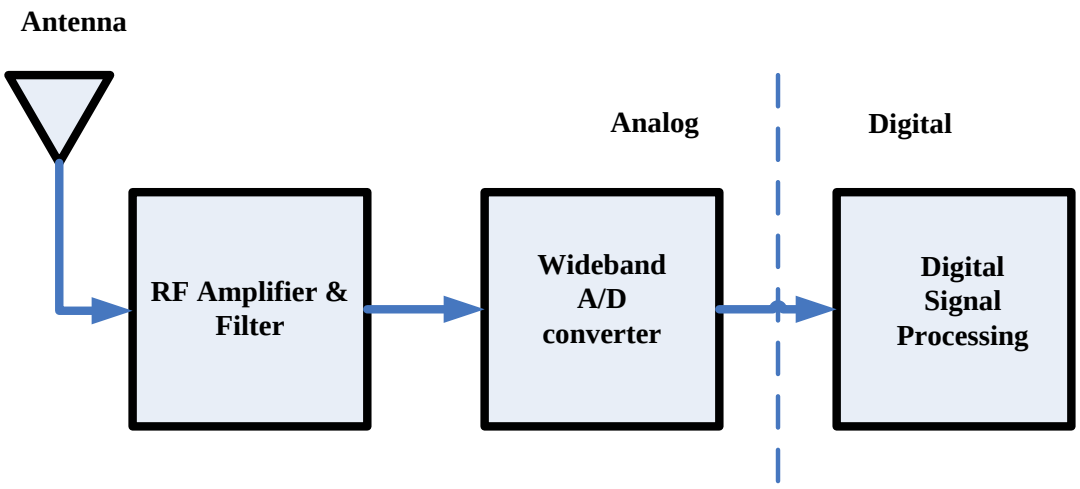

Figure 2.1: The SDR architecture for multi-mode, multi-band transceiver [4].

Figure 2.1 shows the functionality of SDR with realized by software performing signal processing tasks in the digital domain. Not only processing analog radio frequency (RF) signal to cut off channel or band and eliminate noise from adjacent bands, the application of SDR is also to convert the wireless signal to digital data streams at the first stage [4]. By using power digital signal processing (DSP), more flexible software-defined functions and hardware configuration will produces.

Software radios have significant utility for the military and cell phone services, both of which must serve a wide variety of changing radio protocols in real time. In the long term, SDR is expected by its proponents to become the dominant technology in radio communications.

2.2 Architecture of SDR

There are three main functional blocks of the basic digital radio system. It consists of RF section, intermediate frequency (IF) section and baseband section. The RF section consists of essentially analog hardware modules while IF baseband sections contain digital hardware modules [5] which typically been implemented in hardware such as mixers, filters, amplifiers, modulators/demodulators, detectors and etc. are as alternative implemented using software on a personal computer or other embedded computing devices. The concept of SDR is not new, but the rapidly evolving capabilities of digital electronics are making practical many processes that were once only theoretically possible.

A basic SDR may consist of a computer equipped with a sound card, or other analog-to-digital converter, preceded by some form of RF front end. Significant amounts of signal processing are handed over to the general purpose processor, rather than done using special-purpose hardware. Such a design produces a radio that can receive and transmit a different form of radio protocol (sometimes referred to as a waveform) just by running different software.

2.3 Operating Principles and its Ideal Concept

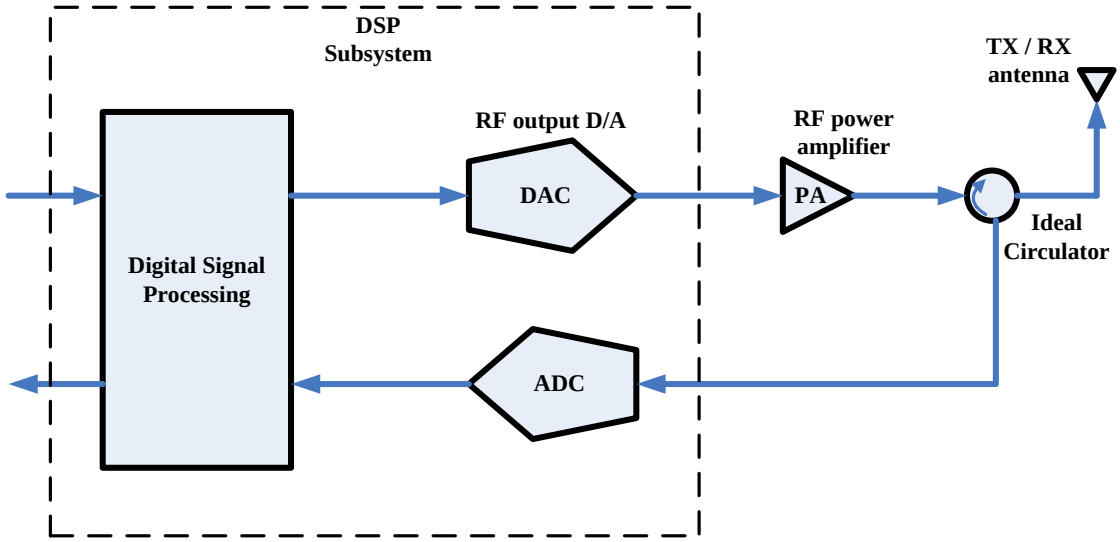

Figure 2.2: Ideal SDR Architecture [6].

Ideally, refer to Figure 2.2; the SDR will have the analog to digital conversion to take place after the antenna. This will leave the subsequent process is carried out in software to transform the stream of data from the converter to any other form the application requires. Conventionally circulator method is used for isolating the transmitting and receiver parts of the transceiver [6].

A digital signal processor would read the converter, and then its software would transform the stream of data from the converter to any other form the application requires. An ideal transmitter would be similar. A digital signal processor would

generate a stream of numbers. These would be sent to a digital-to-analog (DAC) converter connected to a radio antenna.

The drawback of this architecture is the entire RF spectrum is converted by the analogue-to-digital converter (ADC). These results the specification of this device such as bandwidth, dynamic range, and sampling rate is unrealizable.

2.3.1 Receiver Architecture

Most receivers utilize a variable frequency oscillator to tune the desired signal to a common intermediate frequency or baseband, where it is then sampled by ADC. However, in some applications it is not necessary to tune the signal to an IF and the RF signal is directly sampled by the ADC which is take place after amplification.

To achieve a multi-mode and multi-standard receiver, the requirement must be satisfied is broadband and multi-band RF stage, low cost, size and power consumption, and the receiver is compatible with DSP. To reach these goals, the RF stage architecture must be chose accurately. This is because of the conventional super-heterodyne architecture is not a suitable solution to satisfy these requirements such as requirement to several image rejection filters to eliminate images responses due to several bands. This problem can be solved by direct conversion architecture because they have no image response, and thus they do not required any image rejection filters [7].