HIGH SPEED ADDER

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Bachelor of Engineering with Honours
(Electronics and Telecommunications Engineering)
2008/2009

UNIVERSITI MALAYSIA SARAWAK

R13a

BORANG PENGESAHAN STATUS TESIS

Judul: **HIGH SPEED ADDER**

SESI PENGAJIAN: 2008/2009

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Title : High Speed Adder

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has been read and approved by:

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Mr. Nurhuzaimin Julai Date

(Supervisor)

HIGH SPEED ADDER

DAGRIOUS ANAK JIHOB

This project is submitted in partial fulfilment of
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Dedicated to my beloved parent, family members and friends who was supported and encouraged me

Thank you for all the support and encouragement

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ABSTRAK

Terdapat beberapa jenis kumpulan rekaan penambahan di bawah keluarga rekaan penambahan berkelajuan tinggi. Setiap kumpulaan ada kelebihan dan kebaikan tersendiri. Untuk projek ini, tiga ciri-ciri penambah berkelajuan tinggi akan di bandingkan dan dinilaikan dari segi saiz bit, keluasan rekaaan dan perlengahan masa. Matlamat projek ini adalah untuk mereka salah satu kumpulan dari keluarga penambahan berkelajuan tinggi menggunakan perisisan komputer yang berkaitan. Jadi, kemampuan untuk cara mencipta Penambahan Berkelajuan Tinggi yang dipersembahkan dalam projek ini akan dibuktikan. Kepekaan dalam perlengahan masa untuk membezakan proses dan pelbagai persekitaran telah disentuh dengan lebih lanjut dalam perlaksanaan keputusan. Oleh itu, daripada keputusan eksperimen menunjukkan bahawa elemen Penambah Berkelajuan Tinggi mampu memberikan jumlah perlengahan masa yang dapat diterima tanpa menggunakan kuasa yang besar. Dengan itu, daripada perbandingan keputusan yang akan ditunjukkan dalam projek ini nanti akan membuktikan bahawa memilih elemen perlengahan masa yang terbaik adalah sangat berguna untuk diaplikasikan di mana keperluan dalam bentuk masa itu sendiri beroperasi ke arah rekaan penambahan berkelajuan tinggi.

ABSTRACT

There are various group of adder design under high speed adder family design. Each group has its own advantages and disadvantages. For this project, three important criteria of high speed adder will be compared and analyzed: bit size, design's area, and propagation delay. The aim of this project is to design one group member of high speed adder's family using related software. Thus, the capability for the methodology by designing the Brent Kung Adder(s) is presented in this project by which to proven. The sensitivity of the delay elements to different process and environmental variations is studied from the simulation results. Therefore, the experimental result represent that the high speed adder elements gave a reasonable amount of delay without large power costs. So, from the comparison results presented in this project will prove useful for selecting the best delay element to apply which is the essential part for self-timed operation in high speed adder.

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IC	-	Integrated Circuits
CPU	-	Central Processing Unit
ALU	-	Arithmetic Logic Unit
HSA	-	High Speed Adder
FA	-	Full Adder
HA	-	Half Adder
RCA	-	Ripple Carry Adder
CLA	-	Carry Lookahead Adder
PPA	-	Parallel Prefix Adder
BKA	-	Brent Kung Adder
KSA	-	Kogge-Stone Adder
C_i	-	Carry in
C_o	-	Carry out
S	-	Sum
PFA	-	Partial Full Adder
G_i	-	Generates function
P_i	-	Propagate function
L	-	Number of lookahead levels in the design
FPGA	-	Field-Programmable Gate Array
LUTs	-	Slice Look-Up Tables

€	-	Carry Operator
PG	-	Propagate-Generate function
FCO	-	Fundamental Carry Operator
ppC	-	parallel prefix Carry
ppS	-	parallel prefix Sum
CPLD	-	Complex Programmable Logic Devices
EDA	-	Electronic Design Automation
LPM	-	Library of Parameterized Modules
IP	-	Intellectual Property
EDIF	-	Electronic Design Interchange Format
SDC	-	Synopsys Design Constraint
GUI	-	Graphical Unit Interface
SRAM	-	Random Access Memory
t_{pd}	-	Propagation delay

CHAPTER 1

INTRODUCTION

1.0 Background

Computers, mobile phones, gaming devices or consoles, mp3 players, televisions, digital cameras, digital watches and ATM machine are the few types of technology that may came across almost every day. This technology operates with functions of the Central Processing Unit (CPU) or some of it may as simple Integrated Circuits (IC). Generally, the very basic component of either CPUs or ICs is the adder.

The search for hardware algorithms for addition has been started around year 1950. The addition function is the most basic and commonly used arithmetic operation in our life. In terms of digital electronic engineering, adder is a device that will perform the additional operation. Adder is a part of Arithmetic Logic Unit (ALU) in the computer and some ALUs may consist of multiple adder. Adder performs addition operation by using interior combination of primitive logic gate inside adder itself.

Although adder can be constructed in many other numerical representation but basically in computation adder is operated on the binary representation.

As shown in Figure 1.1, the datapath of IC design, one of the very basic structure implemented in IC design in Adder. Adder is widely used in the generic computer [2] for the reason that it is very important for adding data in the processor. The processing speeds of one's computer turn out to be the most considerable requirement acquired by ones technology users.

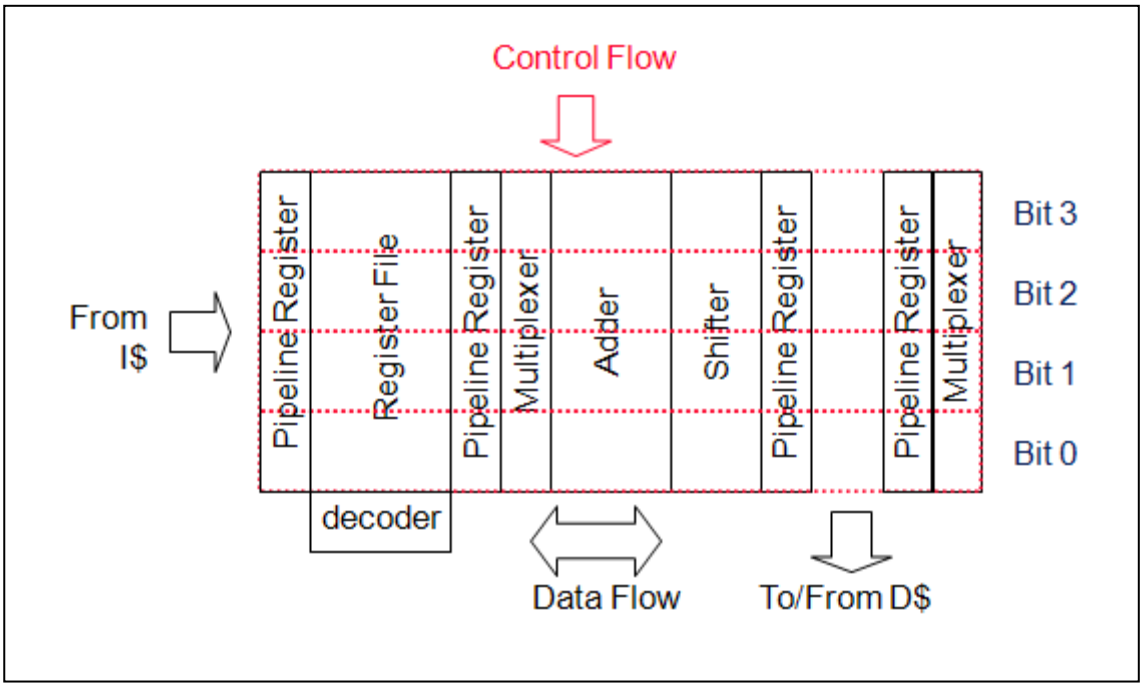

Figure 1.1: Datapath Bit-Sliced Organization in IC designs

In general, the purpose of adder designed is to strive with the Sum operation of the Arithmetic Logic Unit (ALU). This operation is then applied to other arithmetic operation such as: the subtraction, multiplication and the division function. These were very basis operation in order to constructs programs which later are derived into more advance and complex programs which alter into all technology which have been seen nowadays. The performance and the reliability is the main key in order ones technology to be acknowledge these days. As time passed by, the technology operation needs to undergo with smoothly and efficiently. Time is Gold, even a delay of 1 second could cost gargantuan losses, therefore to human always rushing for time, especially for technology devices user, always demanding for the faster speed of technology.

1.1 Objectives of Project

Following are the objective of this project;

1. To design a group of adder which are belongs to High Speed Adder family
2. To design the High Speed Adder group with Quartus II program.
3. To designs and simulates several bit size of High Speed Adder.

1.2 Project Outline

The target of this project is to design a High Speed Adder with Quartus II Web Edition Version 8 program. The Quartus II program is chosen because it includes all of the design files, software source files, plus other related files that necessary for the eventual implementation of a design in a programmable logic device.

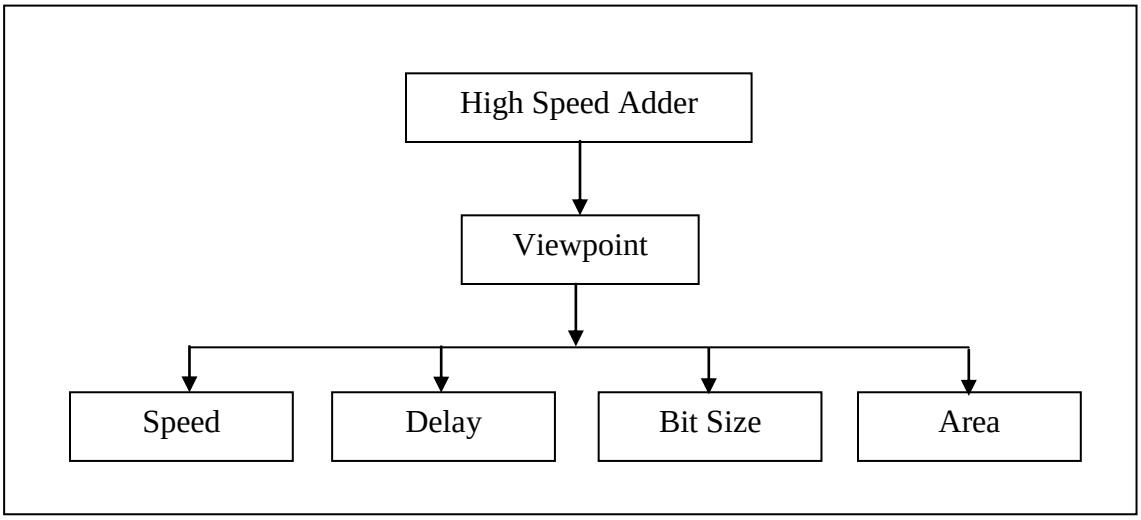

Figure 1.2: Evaluating High Speed Adder Block Diagram

Since there are various type adder design categorize as High Speed Adder, relevant evidence are acquired via comparing and evaluating each adders design in the following viewpoint; intentional output speed, delay, bit size and area. The involvement of bit size will concern in term of cost nowadays. The speed of the output and the delay

point of view isthe verification of performance and the value of the design. While, bit size are the requirement aspect in performance view whereas the design area is a factor of reliability revelation.

As well, the circuitry design areas are also anxiety of the all cost design. All these criteria agonize whether it worthwhile to acknowledge as HSA as well in the price market nowadays. Afterward all the characteristics of high speed adders are compared and the ones with greater advantage is agonize as HSA.

1.3 Thesis Outline of Project

This project is divided into 5 chapters in general and is prearranged as follows:

Chapter 1 of this project report are discusses on the introduction of the Adder operation and the overview of the various types of adder design. In addition, this chapter stated clearly the type of adder design to be research on. Plus, it also included a viewpoint of the adder to be designs. Furthermore, the objective of this project will be included to give a clear view and information needed.

Chapter 2 is the literature review of this project. There various type of High Speed adder design as High speed adder is design stage by stage, starting with HA or FA

design stage until PPA design stage. Each design stage is review in the chapter. The characteristics of a good performance of the High Speed Adder included.

Chapter 3 discusses the study of one type of High Speed Adder; it includes the algorithm of the High Speed Adder. In addition, this chapter also contains the performance comparison of each adder designed. Furthermore a revision method that used in Chapter 1 and 2 is also included. Plus, the methodology of designing project is also affirmed.

Chapter 4 contains the simulation results and a discussion which is comparison and analysis of the delay element are made. Concern the approach and analysis to achieve the objectives.

Chapter 5 concludes and summarizes the overall process and performance of the project. In addition, further work which can be implemented or improve the project is also being discussed for future improvement.