Faculty of Engineering

Formulation and Mitigation of Soft Error in CMOS Memory System by using Transmission Gate

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DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Malaysia Sarawak. Except where due acknowledgements have been made, the work is that of the author alone. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

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ABSTRACT

The downscaling of technology has resulted in increased packing density in CMOS technology and thus, a worrying uptick in single event upset susceptibility in contemporary technology. SRAMs in particular, which now occupy up to 70% of all chip size, are vulnerable to errors from single event upsets, leaving the reliability of its memory storage potentially compromised. The application of submicron electronics in areas of high particle activity in fields such as aerospace calls for the need for technology that is resistant against the occurrence of soft errors, with an increased capacity of mitigating the phenomenon of single event upsets. The current literature has proposed methods such as radiation hardening through methods such as transistor sizing and triple modular redundancy which are unable to keep pace with technology downscaling. This study aims to characterize and model the transient pulse formed from a single event upset, formulate the probability of a state flip in various SRAMs, and produce a transient filter based on transmission gate. The transient pulse, modelled by the double exponential model is injected into the vulnerable memory nodes of the interlocked inverters, Q and QB in the 4T, 6T and 9T SRAMs to observe the amplitude of transient pulse required to incite a state change. The critical charge is then calculated from the readings, and its subsequent probability is calculated further based on the memory node area, technology node of 180nm and the atmospheric cross section per unit area constant. The transmission gate transient filter SRAM achieves an 88% improvement in error probability reduction.

Keywords: Soft error, single event upset, single event transient, SRAM, CMOS

Formulasi Dan Mitigasi Gangguan Ralat Lembut dalam Teknologi CMOS dengan Penggunaan Suis Pemancar

ABSTRAK

Penskalaan semula teknologi telah menyebabkan peningkatan ketumpatan pembungkusan dalam teknologi CMOS dan seterusnya, peningkatan yang membimbangkan dalam kerentanan terhadap gangguan peristiwa tunggal (single event upset, SEU) dalam teknologi kontemporari. SRAM khususnya, yang kini merangkumi sehingga 70% daripada saiz cip keseluruhan, adalah terdedah kepada ralat akibat SEU, sekali gus menjejaskan kebolehpercayaan penyimpanan memorinya. Penggunaan elektronik submikron dalam kawasan yang mempunyai aktiviti zarah tinggi seperti dalam bidang aeroangkasa memerlukan teknologi yang tahan terhadap berlakunya ralat lembut (soft errors), dengan keupayaan untuk mengurangkan fenomena SEU. Literatur semasa telah mencadangkan kaedah seperti pengerasan terhadap sinaran (radiation hardening) melalui teknik seperti penyesuaian saiz transistor dan redundansi modul (triple modular redundancy), namun kaedah-kaedah ini tidak mampu menyaingi kadar penskalaan teknologi yang semakin pesat. Kajian ini bertujuan untuk mencirikan dan memodelkan denyutan sementara (transient pulse) yang terhasil akibat SEU, merumuskan kebarangkalian perubahan keadaan (state flip) dalam pelbagai jenis SRAM, dan menghasilkan penapis denyutan sementara berasaskan gerbang penghantaran (transmission gate). Denyutan sementara yang dimodelkan melalui "double exponential model" akan disuntik ke dalam nod memori yang terdedah pada penyongsang terkunci (interlocked inverters), iaitu Q dan QB dalam SRAM 4T, 6T dan 9T untuk memerhati amplitud denyutan sementara yang diperlukan bagi mencetuskan perubahan keadaan. Cas kritikal (critical charge) kemudiannya dikira daripada bacaan tersebut, dan kebarangkalian berikutnya dikira berdasarkan luas nod *memori, nod teknologi 180nm dan pemalar keratan rentas atmosfera per unit luas. Penambahbaikan kebarangalian sebanyak 88% telah dicapai oleh kaedah yang dicadangkan.*

Kata kunci: *"Soft error", "single event transient", "single event upset", SRAM, CMOS*

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LIST OF ABBREVIATIONS

SER	Soft error rate
CMOS	Complementary metal oxide semiconductor
UNIMAS	Universiti Malaysia Sarawak
BPSG	Borophosphosilicate glass
SRAM	Static random access memory
SNM	Static noise margin
SEU	Single event upset
Q_{col}	Collection charge
Q_{crit}	Critical charge
4T	Four transistor
6T	Six transistor
9T	Nine transistor
C_{node}	Node capacitance
LET	Linear energy transfer
V_{DD}	Supply voltage
MOSFET	Metal oxide semiconductor field effect transistor
NMOS	N-channel MOSFET
PMOS	P-channel MOSFET
WL	Word line
BL	Bit line
BLB	Bit line bar
FF	Flip flop

VTC	Voltage transfer characteristics
I_{read}	Read current
V_{BL}	Bit line voltage
C_{BL}	Bit line capacitance
MCU	Multiple cell upset
MBU	Multiple bit upset
FPGA	Field programmable gate array
LUT	Look up table
V_{th}	Threshold voltage
PR	Pull up ratio
CR	Cell ratio
CNT	Carbon nanotubes
SEE	Single event effects
BEOL	Back end of line
L_f	Length of funnel
TCAD	Technology computer aided
TID	Total ionisation dose
FET	Field effect transistor
TMR	Triple modular redundancy
TPDICE	Triple path dual interlocked storage cell
SOI	Silicon on insulator
HVPDH	Horizontal vertical parity and diagonal Hamming
PIM	Processing in memory
LRS	Low resistive state
HRS	High resistive state

TTF	Transient transmission filter

LIST OF SYMBOLS

τ_α	Collection time constant
τ_β	Ion track establishment time constant
k	Boltzmann constant
ε_o	Permittivity of vacuum
ε_r	Relative permittivity of silicon
q	Electron charge
N_D	Donor density
μ	Electron mobility
τ_r	Rise time
τ_f	Fall time

CHAPTER 1

INTRODUCTION

1.1 Study Background

The downscaling of electronics into the submicron range has presented an old challenge with a new problem, mitigating circuitry against errors with the added issue of single event upsets. If complementary metal oxide semiconductor (CMOS) technology is to obey Moore's law, new design approaches must be taken to continue its trend. The downscaling of technology leads to higher circuit density on a smaller area, leading to higher sensitivity to soft errors occurring.

The study of soft errors has been as a phenomenon has been undertaken since the 1970s when it was first observed to occur in space equipment. Since then, the attention of the scientific community on soft errors has only grown as recent technology trends towards higher sensitivity, especially in SRAMs where downscaling was done by implementing smaller capacitance with smaller dimensions. Now that the trend involves the reduction of transistor dimensions, supply voltage reductions along with a plethora of other parameters, single event transients, once an abstract concept, now present a concrete threat to the continued reliability of CMOS technology. Bolstering CMOS technology against soft errors while simultaneously maintaining the trend of downscaling presents a unique challenge to designers.

Soft errors may be produced when a radiation-sourced particle collides with a gate. While single event transients are temporary in nature and can be overwritten by the next clock cycle, if the transient signal is latched into a memory element, it will lead to the occurrence of a soft error. Soft errors can threaten the reliability of high-performance chips despite their transient nature, exacerbated by the recent prominence of single event multiple transients caused by the upward trend of circuit density (Evans et al., 2016).

The mechanisms of single event upsets and an overview of techniques used for mitigation against them are explored in chapter two. Chapter three covers the methodology used to investigate the soft error sensitivity of the 4-transistor, 6-transistor and 9-transistor static random-access memory (SRAM). In chapter 4, the results of the simulation obtained are discussed and elaborated upon.

1.2 Problem Statement

The field of soft errors is lacking in a method to formulate probability of known vulnerable nodes being affected by soft errors. This study proposes not only a mathematical algorithm to formulate probability, but also a dataset for the SRAM memory response to parameter variations in temperature and voltage supply. SRAMs can experience an increase in the rate of soft errors due to the influence of atmospheric neutrons (Burnett et al., 1993). These soft errors can affect the interlocked inverters holding the data of the SRAM and cause a bit flip to occur (Bota et al., 2009). Not only does the threat to this region need to be analysed, but the SRAM must also have a system in place to protect it against further single event transients that can be scalable with voltage as voltage scaling is one of the first parameters altered in order to reduce the power consumption of a design. This is disastrous in circumstances of where reliability is especially required such as aerospace or in the medical field (Toghuj, 2020; Zhao et al., 2022)

The issue of soft errors has been brought to the forefront of many design considerations as the downscaling of technology in accordance with Moore's law begins to tread the territory of submicron levels (Arden, 2002; Schaller, 1997). With this issue, it becomes imperative that to design qualitative measures to evaluate the robustness or weakness of circuitry to the effects of single event upsets. High density memory devices are especially prone to radiation induced errors, but the severity of soft errors has become has worsened with downscaling and an understanding of soft error probability must be achieved to ensure the reliability of a system against single event upsets. Therefore, theoretical modelling and soft error analysis is crucial to further the understanding of system mitigation and improving the system reliability. Thus, alternative methods for the evaluation of failure probability due to single effect upsets are required to provide a larger selection of tools toward the effort of improving robustness against soft errors.

Though there are existing methods in the field of microelectronics that address these issues mainly in the form of error correction code, radiation hardening by design and the use of triple modular redundancy, further research must be conducted to directly target these erroneous data flips. In the case of this study, the modelling of the transient error using the double exponential model and the subsequent formulation of failure probability based on the 180nm technology node serves to present a novel and realistic mathematical model to represent the robustness of a given system against single event upsets. Furthermore, the study seeks to present a novel method to filter the transient currents from the data nodes of a static random access memory cell, thus avoiding the occurrence of an unintended data flip, a method that provides additional robustness in exchange for minimal area overhead.

1.3 Hypothesis

The critical charge of the SRAM memory node can be increased and therefore hardened against single event upsets through the use of transmission gate transient filters, the results of which can then be validated through a novel method of probability formulation.

1.4 Objectives

The research aims to formulate the probability of the occurrence of a soft error and design a mitigation method against it. This can be achieved through the following set of objectives:

i. To assess the reliability of the circuit and the system due to the SEU

ii. To formulate the probability of soft error when transient current is injected into the system

iii. To mitigate the system with the use of a transmission gate transient filter

iv. To evaluate the performance of the transmission gate transient filter using the probability formulation

1.5 Project Scope

The scope of this project is to investigate a new method with which to evaluate the robustness of a system against data corruption, specifically from the production of a transient current from the single event upset phenomenon, which is produced as a result of an ionised particle impacting the sensitive nodes of an SRAM cell.

The research will be conducted under simulations performed in Cadence Virtuoso version IC5141USR3 wherein the 4T, 6T and 9T SRAMs will be modelled within the analog environment tool using 180nm PDK. The transient current model employed will be based on the double exponential model, which will play a part in simulating the effects of single event upset on the memory nodes of the SRAM cells. The critical charge of the memory node of each SRAM will be acquired and subsequently used to calculate the data flip probabilities for each instance. An additional mitigation measure using transmission gate transient filters will then be proposed and its performance compared against the conventional architectures of the 4T, 6T and 9T SRAM.

CHAPTER 2

LITERATURE REVIEW

2.1 Overview

Current literature on the mechanisms, sources and modelling methods of soft errors is detailed in this literature review. Also included in this chapter are common measures put into place to mitigate, detect, and correct soft errors caused by single event upsets.

2.2 Soft error in CMOS SRAM

SRAM cache is comprised of an array of bi-stable memory bitcells and other circuits. Read and write processes are facilitated by the surrounding circuitry. A conventional SRAM memory architecture is shown in Figure 2.1. An SRAM array is made up of millions of uniform bitcells. Consequently, much research has been invested in bitcell design improvement as any upgrade in reliability, performance and saving in static power has an overall effect on the entirety of the system. High performance processors prioritise operating speed and bitcell area to maintain high cache density and reliability but energy efficiency and reliability present significant issues in low energy applications. A memory bitcell can store a bit of data, either "1" or "0" (J. Singh et al., 2013).

The columns of each SRAM array share a word-line (WL) and a pair of bitlines (BL, BLB). SRAM arrays are bound by the bitline and word-line capacitances and resistances. SRAMs are used in cache memories and systems-on-chip (SOC) to take advantage of their superior speed. Device scaling, however, poses design challenges. Now designers must work around lower threshold voltages and specified manufacture conditions put in place to reduce energy leakage.