

Evaluating NoC and WiNoC Architectures for Multicore Architecture Performance

Asrani Lit

Faculty of Engineering

Universiti Malaysia Sarawak (UNIMAS) Universiti Malaysia Sarawak (UNIMAS) Universiti Malaysia Sarawak (UNIMAS)

Kota Samarahan, Sarawak

lasrani@unimas.my

Nazreen Junaidi

Faculty of Engineering

Kota Samarahan, Sarawak

jnazreen@unimas.mymy

Shamsiah Suhaili

Faculty of Engineering

Kota Samarahan, Sarawak

sushamsiah@unimas.my

Shirley Rufus

Faculty of Engineering

Universiti Malaysia Sarawak (UNIMAS)

Kota Samarahan, Sarawak

rshirley@unimas.my

Nor Asrina Ramlee

School of Engineering & Technology

University of Technology Sarawak

Sibu, Sarawak

asrina@uts.edu.my

Fariza Mahyan

Department of Electrical Engineering

Politeknik Kuching Sarawak

Kuching, Sarawak

fariza.m@poliku.edu.my

Abstract—To mitigate potential scalability challenges in future many-core architectures' on-chip communication systems, the wireless Network-on-Chip (WiNoC) design concept has arisen as a compelling choice. It offers a viable approach to address these issues effectively. This paper delves into an extensive analysis of the performance evaluation concerning Network-on-Chip (NoC) and Wireless Network-on-Chip (WiNoC) configurations within the framework of a 64-core multicore system. The study encompasses a thorough evaluation across four synthetic traffic profiles, namely random, shuffle, butterfly, and transpose traffic distributions, offering a comprehensive understanding of their impact on system performance. This evaluation involved a thorough analysis of data transmission latency, the efficiency of network data throughput, and the amount of energy consumed. In order to substantiate our conclusions, we conducted simulations encompassing the 64-core mesh-based NoC and WiNoC architectures. These simulations were executed utilizing the Noxim simulator, a well-recognized tool acclaimed for its capacity to provide cycle-accurate simulations. Analyzing the simulation outcomes, it becomes evident that the 64-core WiNoC architecture performs better in terms of network performance. This is evident from its ability to handle heavier workloads and achieve lower delays in all traffic situations, when compared to the 64-core NoC architecture.

Index Terms—Wireless Network-on-Chip, Performance Evaluation, Multicore, Traffic Distribution

I. INTRODUCTION

In recent decades, on-chip interconnect architectures have emerged as feasible communication solutions for chip multiprocessors. This trend is supported by research studies like [1]–[3]. Recent advancements in silicon chip technology have made it possible to create integrated chips with up to hundreds processing cores. Numerous chip prototypes have been developed and utilized in various projects, featuring Network-on-Chip (NoC) architectures with multicores. Notable examples include TILERA [2], RAW [4], SCORPIO [5], and Xeon Phi [6].

The challenge posed by wire delay is significant in chip-based network architecture, especially while addressing expansive on-chip communication systems, as it can significantly affect the entire network capabilities and performance [7], [8]. As quantity of processing cores continues to grow, the traditional wired NoC architecture faces limitations due

to its dependence on long-distance multi-hop communication. Consequently, this results in an architecture that use more power and demonstrates increased latency. Therefore, to tackle challenges related to elevated latency in signal propagation and long-distance multi-hop communication between processing cores, computer architects and researchers have introduced the design of Wireless NoC (WiNoC) interconnect as a viable solution [9]–[12].

In order to facilitate communication over long distances among computing cores, this method requires the incorporation of one-hop wireless transmission [13]–[18]. The WiNoC infrastructure includes an integrated transceivers that enables the creation of an immediate wireless medium for packet transmission throughout the on-chip interconnects, especially across far distances [14], [19], [20]. The key network characteristics of the WiNoC architecture, including its topological organization, data flow governance, and routing system have a substantial impact on its overall effectiveness as a network system [21]–[25]. Hence, the primary objective of this paper is to evaluate the mesh topological performance of NoC and WiNoC for a network architecture comprising a 64-multicore system.

The paper continues with the structure outlined below, beginning with Section II, that presents an overview of the mesh network topology in the context of NoC and WiNoC architecture. In Section III, we outline the configuration employed in the simulation based on Noxim. The following section IV showcases the simulation results and offers the critical analysis. In conclusion, Section V summarizes this paper and provides some suggestions for future research directions.

II. MESH-BASED NETWORK ARCHITECTURE

WiNoC is a an extension interconnect for NoC, offers a solution to mitigate the significant transmission latency associated with conventional wired communication by integrating both wired-wireless connections in establishment of efficient wireless communication communication [13]–[18], [26]–[28]. Furthermore, due to the progress in on-chip radio transceivers

integration [19], [20] and the compatibility if the CMOS mm-wave antennas [29], [30], the WiNoC design has emerged as a possible improvement for the conventional NoC system [31].

The topological structure used for connecting components in a WiNoC has a critical influence on the architectural cost and system's performance. Therefore, it becomes a crucial aspect to take into account throughout the designing phase. Key factors affecting the design of a WiNoC architecture involve various aspects such as the interconnections among processing IP cores, encompassing the physical layout, , and transceiver design [32]–[34].

Figure 1 illustrates the 8×8 multicore mesh-based on-chip network. By integrating radio transceivers into the NoC tiles, it allows for wireless communication between IP processing cores located at considerable distances proximity from each other directly, leading to single-hop wireless connectivity for WiNoC.

III. CONFIGURATION FOR EXPERIMENTAL SIMULATION

The study employed Noxim [35], a Network on-chip simulator with cycle-level accuracy, to evaluate the performance of the 64-core NoC and WiNoC architectures under investigation. The simulator's capabilities include the ability to enable wireless transmission in a mesh-based multicore configuration using a XY wormhole based routing approach. This Noxim simulator precisely replicates the delay in routing crossbar arbitration and path selection, utilizing real values derived from a router prototype design. The specific simulation configuration settings for this study are detailed in Table I.

TABLE I: Configuration for Noxim Simulation

Configuration	Details
Multicore System	64-core NoC, 64-core WiNoC
Technology	65 nm
Clock Frequency	1 GHz
Simulation Time	100, 000 (cycles)
Wireless Frequency	mm-wave
Wireless Data Rate	16 Gbps
Traffic Distribution	Random, Shuffle, Butterfly, Transpose
Routing Scheme	XY Algorithm

To attain a stable state, every simulation run for both architectures was run for 100,000 cycles. To conduct a comprehensive evaluation, the simulations included various commonly used synthetic traffic patterns, including random, shuffle, butterfly, and transpose traffic.

IV. EXPERIMENTAL RESULT AND ANALYSIS

In this section, we evaluate the performance of the 64-core mesh-based NoC and WiNoC architecture. This assessment considers various synthetic workloads, including random, shuffle, butterfly, and transpose distributions. In order to assess the performance of a system or network, we use specific metrics as indicators of how well it functions. In this context, we evaluate performance using two key metrics: network throughput and communication latency. Additionally, we conducted an analysis of energy consumption for both architectures under various traffic scenarios.

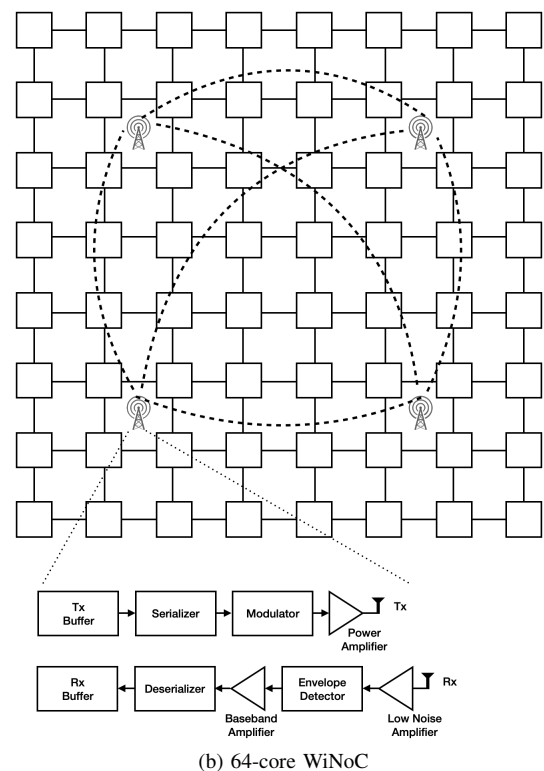
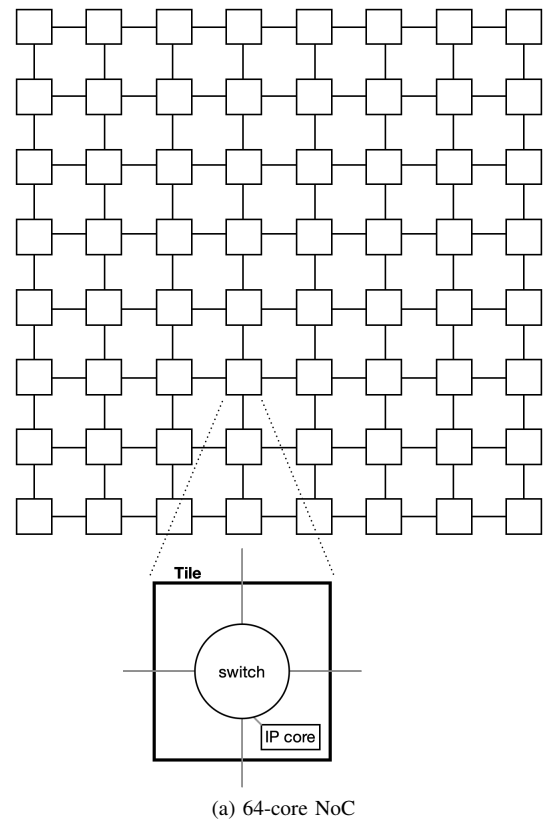


Fig. 1: Multicore mesh network architecture (a) 64-core NoC (b) 64-core WiNoC

A. Communication Latency Implications

Latency is characterized as the cumulative count of clock cycles required for a data packet from its point of IP node, traverse through the multicore network system, and arrive at its IP destination node's position. Figure 2 illustrates the impact of latency for 64-cores NoC and WiNoC architecture under distinctive traffic distributions. The graph illustrates the connection between the injected packet workload and the associated latency measured in clock cycles. It depicts span of latency values, each exhibiting a particular graph curve. As the packet injection rate (PIR) of the provided load increases, the latency steadily rises. However, when operating under higher loads, latency experiences a significant increase with PIR, indicating that the network has reached its maximum load.

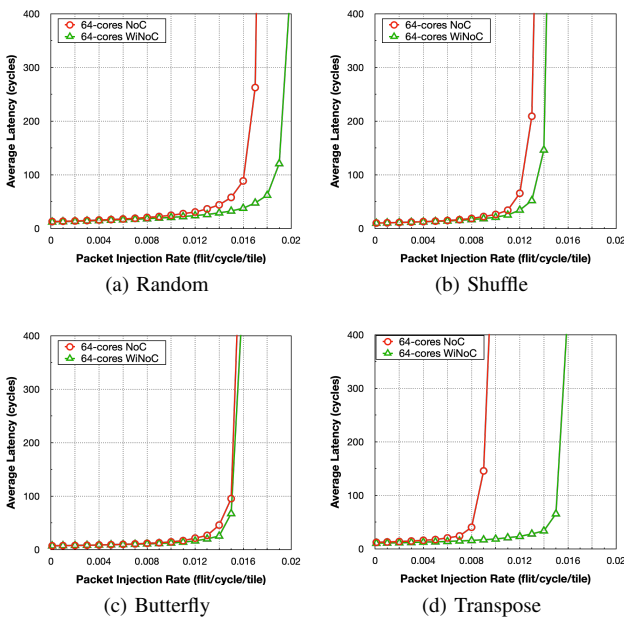


Fig. 2: The impact of latency for 64-cores NoC and WiNoC architecture under various traffic distributions.

Overall, when it comes to traffic distribution, the 64-core WiNoC architecture exhibits better performance in terms of achieving higher PIR (Packet Injection Rate) compared to the 64-core NoC architecture, except in the case of butterfly traffic. In butterfly traffic situations, even though both the 64-core WiNoC and 64-core NoC reach a PIR of 0.014 flit/cycle/tile, the 64-core WiNoC has a faster response time, taking only 67 cycles compared to the 95 cycles needed by the 64-core NoC. It's interesting to note that in the case of transpose traffic, the WiNoC architecture shows a significant increase in PIR, reaching 0.015 flit/cycle/tile, whereas the 64-core NoC architecture only achieves 0.008 flit/cycle/tile.

B. Network Throughput Implications

The network throughput can be described as the speed at the transmission of data packets through the multicore network architecture. Additionally, the concept of saturation throughput refers to the situation when the network demand

reaches its highest point, and the throughput matches the load demand. When the multicore network system attains this state, therefore the network becomes ineffective in efficiently transmitting the generated data packets.

Figure 3 illustrates the impact on network throughput for 64-cores NoC and WiNoC architecture under various types of traffic distribution. This figure shows the fluctuation in network throughput as with the gradual increment of PIR workloads are considered.

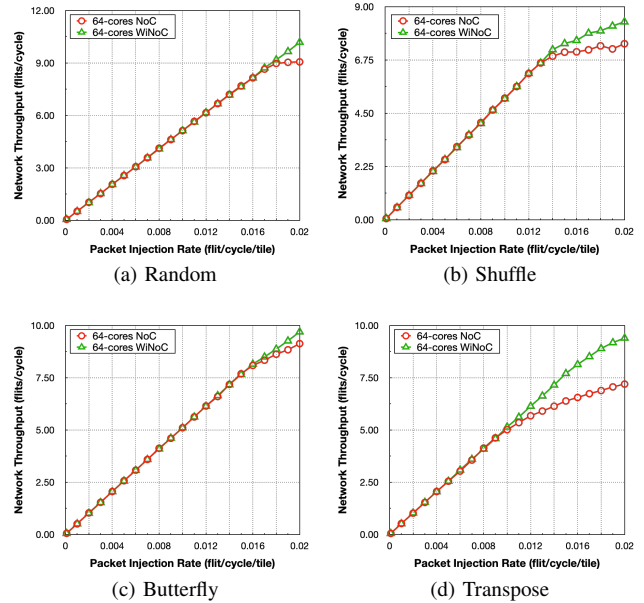


Fig. 3: The implication of network throughput for 64-cores NoC and WiNoC architecture under various traffic distribution.

The experimental findings indicate that the WiNoC architecture with 64-cores consistently delivers higher network throughput across all the examined traffic scenarios. Specifically, it achieves network throughput rates of 9.18 (random traffic), 6.62 (shuffle traffic), 6.65 (butterfly traffic), and 7.7 flits/cycle (transpose traffic). In contrast, the 64-core NoC architecture achieves lower network throughput rates of 8.15 (random traffic), 6.18 (shuffle traffic), 7.18 (butterfly traffic), and 4.13 flits/cycle (transpose traffic) in comparison.

C. Energy Consumption Implications

In the context of a multicore network system, energy consumption means the quantity of electrical power utilized by the several components and executions within the on-chip multicore. Monitoring and managing energy consumption is essential for optimizing network efficiency. Figure 4 shows the implication of energy usage for 64-core NoC and WiNoC architectures under numerous traffic distributions.

In terms of energy utilization, it is evident that the 64-core WiNoC architecture exhibits increased energy consumption primarily attributed to the incorporation of supplementary transceiver components within the WiNoC framework. When the architecture operates at its peak PIR saturation load, the energy consumption values are as follows: 1.52×10^{-4} J

(random), 1.26×10^{-4} J (shuffle), 1.29×10^{-4} J (butterfly), and 1.44×10^{-4} J (transpose), respectively.

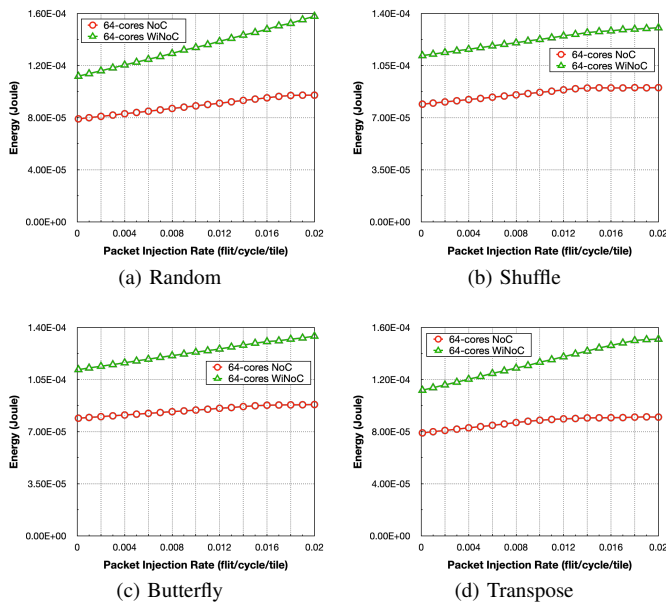


Fig. 4: The implication of energy utilization for 64-cores NoC and WiNoC architecture under various traffic.

V. CONCLUSION

The primary endeavor of this investigation was to conduct a comprehensive evaluation of multicore system performance in the specific context of NoC and WiNoC architectures, both implemented within a 64-core mesh network. This evaluation encompassed the analysis of their behavior under varying synthetic traffic scenarios, including random, shuffle, butterfly, and transpose traffic patterns. The conclusion drawn from the simulation results is that the WiNoC architecture provides better performance, characterized by enhanced capabilities at higher PIR saturation loads, improved network throughput, and minimized latencies. Nevertheless, it is important to note that there is a tradeoff associated with the WiNoC architecture, as it consumes a greater amount of energy. This is primarily attributed to the inclusion of an extra wireless transceiver component, which is utilized for wireless communication purposes. For forthcoming research endeavors, the focus will be on exploring the impact of traffic patterns designed for specific applications' benchmarking, such as SPLASH-2 and PARSEC, within the context of diverse network topologies. These topologies will encompass small-world and honeycomb configurations, allowing for a more comprehensive understanding of network performance dynamics.

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