Design and Analysis of a Practical RMS Power Detector Using Power MOSFET

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Abstract - Power detector chip design and fabrication have experienced significant advancement with the emergence of various technological processes such as BiCMOS and CMOS. With the continuous downscaling of semiconductor devices, chip fabrication has become more complex and less accessible. This paper investigates the design and analysis of RMS power detectors using power MOSFET. A BSIM3 model developed from extracted parameters of the power MOSFET datasheet was employed to design and simulate the RMS power detector. A cascode structure with a current-source load was used to realize high conversion gain and sensitivity. RMS detection is realized by exploiting the square-law principles of MOS transistors in the strong inversion region. The proposed RMS power detector targets practical applications in the agricultural sector and educational institutions. The RMS power detector was fabricated using FR4 PCB substrate. The measurement results at 2 GHz suggest that the RMS power detector employed using power MOSFET on FR4 PCB substrate can detect RF power.

Keywords – BSIM3, impedance matching, power MOSFET, RF circuits, RMS power detector

I. INTRODUCTION

Power detectors are employed in various applications to measure transmitted RF power levels and optimize power consumption [1-3]. Since measuring RF signal power levels has become crucial in recent years, the need for low-cost technologies has exponentially increased the research and development of power detectors. RF signals power levels can be measured using either RMS detection or peak detection [4]. RMS detection is insensitive to Peak-to-Average envelope power Ratio (PAR) and offers better accuracy compared to peak detection. Therefore, RMS detection is more suited for modulated signals with high PAR [1, 5]. RMS power detectors can be implemented using the succeeding approaches: translinear detection [6-8], diode detection [9, 10], and thermal detection [11, 12].

Furthermore, power detectors are usually fabricated using the following technologies: III-V technologies [13], BiCMOS [14, 15], and CMOS [3, 16, 17]. These technologies offer various advantages to chip design which enhance performance. For instance, BiCMOS technology offers excellent noise performance [14, 18], III-V technologies have high electron mobility, and CMOS technology provides ultra-low power consumption and high packing density [1, 19]. Even though most of these technologies offer good performance, such processes’ complexity and cost made their access limited. Furthermore, with the recent increase in the price of chip fabrication, it is crucial for further research on other low-cost design methods to fabricate a practical high frequency RMS power detector suitable for RF signal measurement.

This paper investigates the design and implementation of a practical RMS power detector using power MOSFET for operation at 2 GHz. Power MOSFETs are employed since they are readily available and more practical to implement on PCB substrate than using other technology processes. Since the RMS power detector targets agricultural and educational applications, excellent accuracy is not a critical requirement. Therefore, implementing a practical RMS detector using readily available power MOSFET could benefit applications where minimum costs and shorter fabrication time are more important than maximum accuracy. Section II will describe