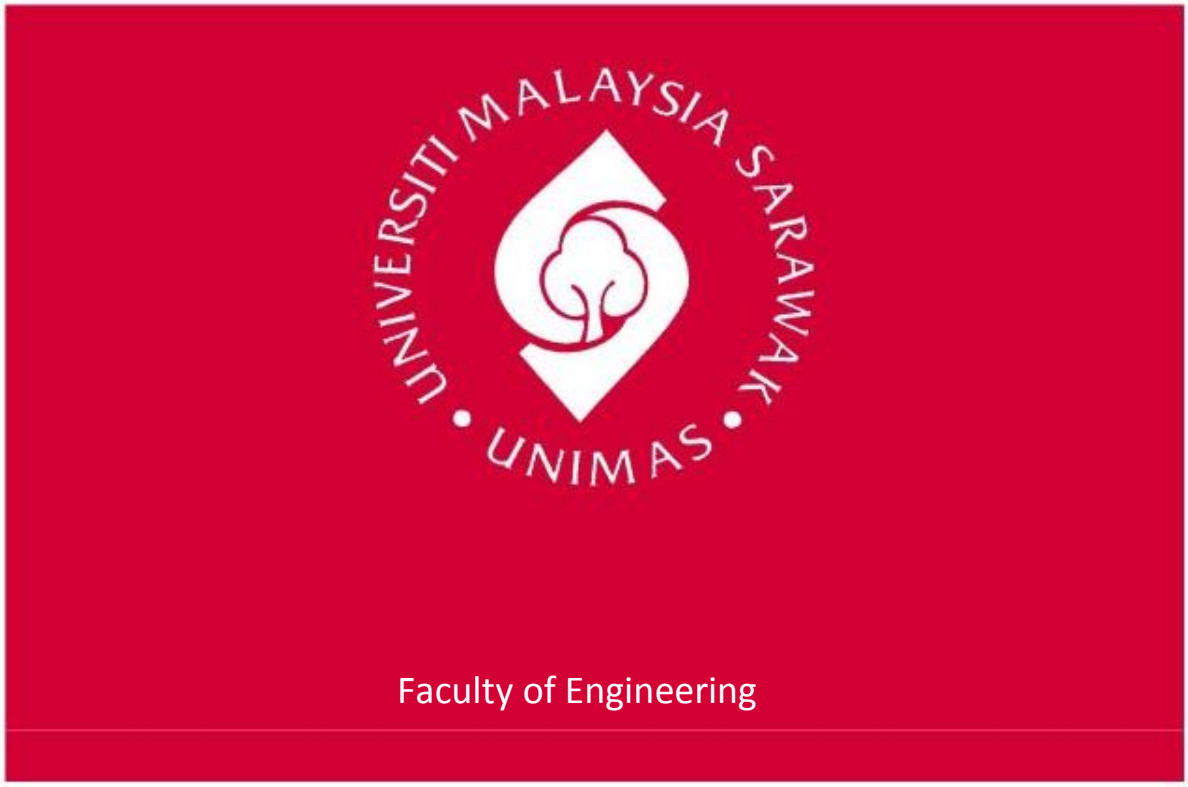

SOFT ERROR IN ASYNCHRONOUS CIRCUIT DESIGN

Dayang Nurul Afiqah Binti Abg Mohd Tahir

Bachelor of Engineering (Hons) in
Electronics (Telecommunications)
2019

UNIVERSITI MALAYSIA SARAWAK

Grade: A-

Please tick (√)

Final Year Project Report ☐

Masters ☐

PhD ☐

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This declaration is made on the 13 day of JUNE 2019.

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Name of the student (Matric No.)

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SOFT ERROR IN ASYNCHRONOUS CIRCUIT DESIGN

DAYANG NURUL AFIQAH BINTI ABG MOHD TAHIR

A final year project report submitted in partial fulfilment of
the requirement for the degree of
Bachelor of Engineering (Hons) in Electronics (Telecommunications)

Faculty of Engineering
Universiti Malaysia Sarawak

2019

To my beloved family and friends

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Thanks for all your encouragement!

ABSTRACT

Soft error considers as a serious concern in state holders as it can cause the circuit to malfunction temporarily. Soft errors are categorised as Single Event Upset (SEU) and Single Event Transient (SET). Radiation actuate soft errors are often happen to most of the electronic products especially with the CMOS technology development. A particle striking on any of the electronic products that can produce soft errors that can be either single event upset or single event transient. Soft errors are not reproducible, and it corrupt the data integrity of the system. This project presents several nodes that are injected with the soft error in the asynchronous circuit. An asynchronous circuit was design using the dual rail encoding and 3-6 code converter while the soft error is represented by using XOR logic gate. The effect of the soft error to the asynchronous circuit is it changed the stored data and it produce errors on the waveform which mean the output parameters are not the same as output parameters. In the project, the presence and absence of error are analysed by observing the output parameter of the waveform that are produced. The software is used to design entry, synthesize the design, compile the schematic diagram, stimulate the gate level schematic of the asynchronous circuit as well as the addition of soft error in the circuit. Moreover, logic gates are commonly used to design the C-element in the software used. The software used to complete the project is Quartus ii Prime Lite edition software.

ABSTRAK

Ralat lembut dipertimbang sebagai perkara yang serius dalam keadaan pemegang kerana ia boleh menyebabkan litar tidak berfungsi untuk sementara. Ralat lembut dikategorikan sebagai Single Kecewa dan Single Sementara. Radiasi menggalakkan ralat lembut supaya sering terjadi kepada kebanyakkan barangan elektronik terutama dengan pembangunan teknologi CMOS. Zarah menarik perhatian mana mana barangan elektronik yang boleh menghasilkan ralat lembut samaada Single Kecewa atau Single Sementara. Ralat lembut tidak boleh dihasilkan semula dan ia memusnahkan integrity data dalam sistem. Projek ini mempersembahkan beberapa nod yang disuntikkan dengan ralat lembut di dalam litar asynchronous. Litar asynchronous telah direka bentuk menggunakan XOR pintu logic. Kesan daripada ralat lembut kepada litar asynchronous ialah ia boleh mengubah maklumat yang telah disimpan dan ia juga akan menghasilkan kesalahan kepada bentuk gelombang dimana ia membawa maksud parameter pengeluaran tidak akan sama dengan parameter input. Di dalam projek ini, kehadiran dan ketiadaan kesalahan adalah dianalisis dengan menilai parameter pengeluaran bentuk gelombang yang dihasilkan. Perisian telah digunakan untuk mereka bentuk kemasukan, mengsintesis reka bentuk, menyusun rajah skematik, merangsang tahap pintu skematik kepada litar asynchronous serta penambahan ralat lembut di dalam litar. Tambahan pula, pintu logic adalah yang selalu digunakan untuk mereka bentuk element C di dalam perisian yang digunakan. Perisian yang digunakan untuk melengkapkan projek ini ialah Quartus ii Prime Lite Edition.

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LIST OF ABBREVIATIONS

BPSG	-	*Borophosphosilicate glass*
CD	-	Code Detector
CMOS	-	Complementary Metal Oxide Semiconductor
CPU	-	Central Processing Unit
DI	-	Delay Insensitive
DRAM	-	Dynamic Random-Access Memory
ECC	-	Error Correcting Code
EDAC	-	Error Detection and Correction
ESD	-	Electro-Static Discharge
FFs	-	Flip- Flops
FSM	-	Finite State Machines
I/O	-	Input/output
IC	-	Integrated Circuit
LET	-	Linear Energy Transfer
NMOS	-	N-type Metal Oxide Semiconductor
PMOS	-	P-type Metal Oxide Semiconductor
QDI	-	Quasi Delay Insensitive
RAM	-	Random Access Memory
SER	-	Single Error Rate
SEU	-	Single Event Upset
SI	-	Speed Independent
SOI	-	Silicon on Insulator
SRAM	-	Static Random-Access Memory

CHAPTER 1

INTRODUCTION

1.1 Introduction

In this chapter, a brief explanation about the project was discussed. Moreover, the problem statement and project objectives were also included in this chapter to give a basic description about the project which entitle "Soft error in asynchronous circuit design". The overview of asynchronous circuit and synchronous circuit were discussed in this chapter.

1.2 Overview

Sequential circuit consists of a combinational circuit which the asynchronous circuit is also known as binary signals but there is no discrete and common time for the signals. This means that, if there are any changes in the input variables, internal states can vary and change at any time.

Unlike synchronous sequential circuits, asynchronous circuit does not have clock signal. It has excellent achievement but difficult to design due to inappropriate timing [1] .

Synchronous circuits used clock pulses to synchronize the data and it is not difficult to design[1]. Moreover, asynchronous circuit's storage elements are connected to form a feedback path. Basically, there are two types of sequential circuits which are synchronous and asynchronous circuit.

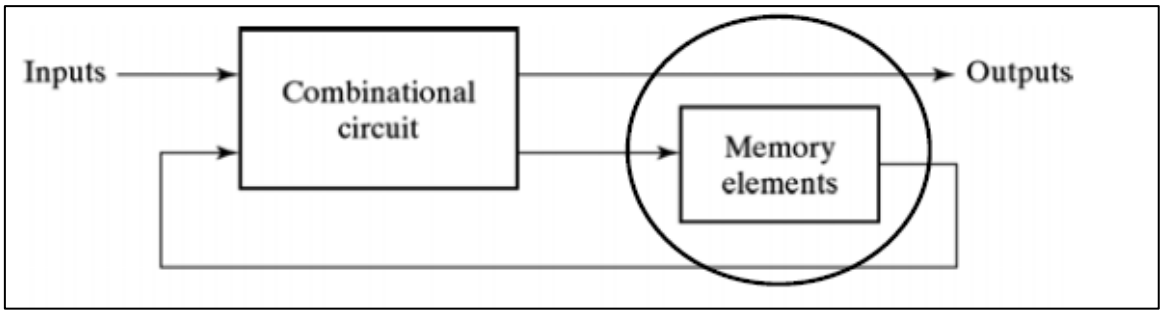

Figure 1.1 Block Diagram of sequential circuit[1].

Figure 1.2 shows the block diagram of sequential circuits which are synchronous and asynchronous circuit. The memory elements are the primary difference in the sequential circuit.

In synchronous circuit, the memory element referred to a clocked flip flop while in asynchronous circuit, the memory element referred as time delay or an unlocked flip flop. One of the strengths of asynchronous circuit compared to synchronous circuit is asynchronous circuit works faster than synchronous because there is no clock used and involved in the circuit[2].

To stimulate asynchronous circuit, a set of unique challenges in stimulating the asynchronous circuit such as detecting hazards, handle sequential behaviour and dealing timing constraints[3].

To perform any synchronization, communication and sequencing of operations, the handshaking between the components is used[4]. In addition, asynchronous design are categories as Delay Insensitive (DI), Quasi Delay Insensitive (QDI) and Speed Independent (SI) circuits [5].

Asynchronous circuit is used when the operation speed is significant where it gives an immediate result without waiting for a clock pulse. Hence, not many components are needed in the circuits and it requires only the important components. Since asynchronous circuit is synchronize naturally, the input signals changes may affect the internal clock [1]. Furthermore, asynchronous circuit is used in the communication between two units with their own independent clocks[1].

In addition, synchronous design is typically flip-flop-based at the micro-architectural level, although latch-based design is quickly gaining value, mainly due to its low-power advantages. Asynchronous and high-performance architecture designs

appear to use data-driven channels with latches embedded with the logic16, while low-power-oriented design styles tend to have more control-oriented architectures with explicit latches [6].

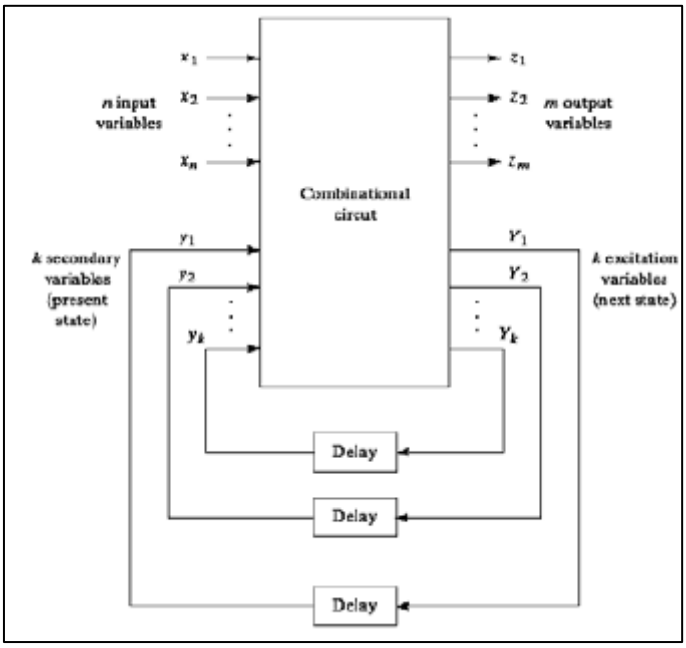

Figure 1.2 Asynchronous sequential circuit[1].

Figure 1.2 shows the asynchronous sequential circuit. From the figure above, it shows that the changes in input variables can affect the internal states at any instant time and there is no clock signal is needed.

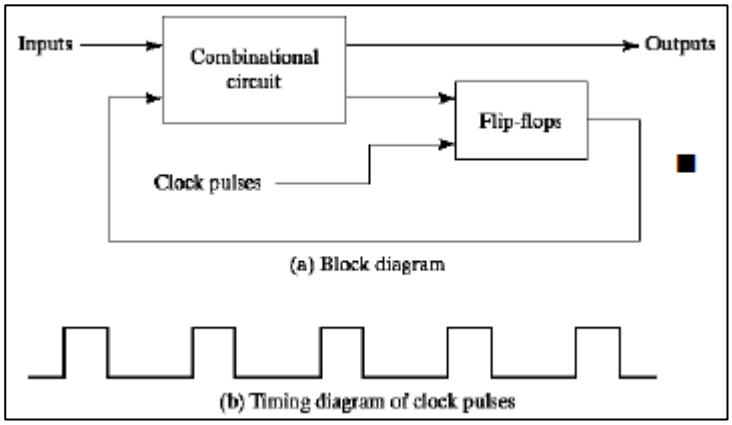

Figure 1.3 Synchronous sequential circuit[1].

As shown in Figure 1.3, synchronous circuit required clock pulse to synchronize by periodic train. In addition, at active stage of the clock, the states of memory will change if the input is change[2].

Soft error may be generated by various cases. The major constancy threat for digital VLSI system is the radiation induces soft errors when the semiconductor device scaling down [7]. The term “soft error” defines to a temporary error that occurs in the semiconductor devices. Soft error occurs because the results of the particles which is alpha particles from packaging or neutrons from atmosphere, hit the structures of the silicon[8].

This caused the state to change the condition from low to high or high to low. Moreover, this electrical effect occurs due to the electron hole pairs was generated in the reverse biased junction of the opposite device[8].

Currently, as the technology nodes of 90nm and below are more practical, transistors come in a very small size[8]. With voltage scaling, the threshold voltage and the drain current are decreased eventually. As a consequent, in the combinational logic, the radiation induced soft errors are increasing attention and will become crucial as directly induced errors for state elements. Previously, the problem of SEU was ignored until the transistors has been scaling and completely reached deep submicron technology.

SRAM and DRAM can be used to figure out the harshness of SEU towards high density in memory devices[8]. In addition, SRAM and DRAM are crucial elements in an advanced IC. SRAM consists of four or six transistors while DRAM consists of single transistor and capacitor. Hence, it makes SRAM less dense compared to DRAM.

Soft errors are known as “glitch” which is commonly found in semiconductor devices. These glitches are does not destroy the device hence it is random, not catastrophic. In CMOS circuit, soft error occurred because of the strikes that hit the charged particle that are exist in the atmosphere as and from the chip itself which is αparticles. In the late 1970s, many attentions of soft error increased by the user and the problem is known is a memory data corruption issue. This is because DRAMs started to apparently be revealed as the form of random failure in CPU.

1.3 Problem Statement

Soft errors commonly appeared in a situation where there is something wrong in the signal or information or signal entered [9]. Currently, not only single bit error, but the

multiple bit errors are already hit most of the electronic devices[10]. Hardware failure happened because of the changed of stored information that is known as soft error or hard error.

Since asynchronous circuit design is used for low power consumption, the soft error needed to be reduced or eliminate to produce a high performance. Hence, soft error is crucial in the research community since in the early 1975s, an aerospace electronics were affected from the radiation[10]. Despite many soft error analysis tools were introduced in a few years to detect the soft error, the experimental soft error injection on the configuration need to be done and analysed.

It is important for future work to analyse the pattern of soft error in order to produce a soft error detection tool. It is to ensure the detection tools produced can detect and analyse the soft error that occurred in most of the electronic devices. To do the research, the details analysis of error propagation at each abstraction level need to be done properly.

1.4 Project Objectives

The objectives obtained for this project are:

1. To design asynchronous circuit design with injection of soft error using Quartus ii Prime Lite Edition software.
2. To analyse the changes of the output waveform of the asynchronous circuit to know the presence and absence of soft error in the system.

1.5 Report Structures

The report features a proposed work, theoretical simulations and any relation to soft error in asynchronous circuit design. This report is divided into five chapters which consisted of introduction, literature review, methodology, research analysis and lastly is conclusion. The report outline for each chapter is as follows:

- Chapter 1 introduces the main objectives of the project which also included the overview and problem statement of the project. Problem statement is the section

where the problems of the project are mentioned. In this chapter also included the project overview which explain briefly about the soft error, synchronous and asynchronous design. Furthermore, the project outline provides information which is delivered via the separate chapters.

- Chapter 2 present the literature review on many aspects of the project such as soft error, Asynchronous design, and different types of Dual Rail data. It gathers all the information needed to accomplish the project. Different perspective and researches about the related title from various researchers or engineers are presented in this chapter to give the best understanding to the readers.

- Chapter 3 provides an explanation on the methodology used in this project through the research process. This is followed by detailed flow charts for the developed project. Then, the design for every pipeline in the asynchronous circuit was also design by using the Quartus ii Prime Lite Edition Software. Hence, the software used to implement the soft error into the Asynchronous circuit design was also been discussed in this chapter.

- Chapter 4 presents the design implementation and result analysis for each part. All the results obtained are shown and explained in detail and well manner. In addition, all the related data, plots and graphs are also inserted to justify the obtained results. The analysis section emphasizes on the analysing circuits, factors that caused the soft error in electronic circuits and the implementation of soft error in asynchronous circuit design. Moreover, all the problems faced in the project that resist from getting the expected results are also discussed in this chapter. The overall results and performance are indicated.

- Chapter 5 concluding the thesis while providing the recommendation for future work. It also concludes the overall objectives and targets that are achieved. The configuration of each design circuit to get the analysis of soft error in asynchronous design limitations are explained well in this chapter. Furthermore, some useful recommendations are given for future works.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this literature review, parts of soft error such as radiation mechanisms in semiconductor and soft error mitigation techniques were discussed. Moreover, the types of SRAM cell also provided in the thesis. The 6T SRAM cell which include the write and read operation also have been discussed in this literature review.

2.2 Soft error

In RAM, there are errors which can cause a temporary condition to the data stored. The errors can change the data that stored in RAM. Two types of the error are either soft errors or hard errors.

In computer industry, the term “soft fail” which mean may be repairable is used to compare between the “permanent fail or hard”. The permanent hardware faults in the electronic circuit may not be able to recognize events and the single bit in the system will change spontaneously and the failure cannot be repeated[11] .

Soft fails or soft error that occurred in most semiconductor memory devices is commonly caused by source of electric noise such as a noise from lighting, power supply, electrostatic discharge (ESD) or thermal radiation from the galaxy such as atmospheric gases and radiation-emitting stars [11]. The frequent factor of soft error in semiconductor memory device is Alpha radiation. In devices of semiconductor memory that are packaged in ceramic, soft errors which can be triggered by way of alpha particles may be reliability situation for microelectronics [11].

Semiconductor memory devices of soft error can occur randomly. The soft errors are reversible and do not involve with any everlasting harm that can happen to the

device. Moreover, the soft error does not continue from the previous process of cycle and the bits that are affected are no more responsive to unsuccessfulness compare to another bit in the device. In semiconductor device, the primary source of alpha particle is the decay of Th232 and U-238 [12].

The decay can be found in certain small amount in the electronic packaging materials. Moreover, the devices are more prone to soft error when the chip on the devices are packed in high density, low scale of geometry devices and the lower power-supply voltage [12]. Currently, major risk to system reliability in deep technologies of sub-micron is known as soft error [13].

2.2.1 Radiation mechanisms in semiconductor

There are three common principal radiation mechanisms that triggered the soft errors in semiconductor devices. The release of alpha particles from semiconductor packaging materials has effect the damage due to the development of electron hole pairs [12]. Uranium and Thorium are radioactive isotopes that contain the highest activity among naturally occurring materials [11]. When the energy state of the unstable nucleus isotope decays decreases, then during radioactive decay , the emission of alpha particles change to high atomic atom when in contact with another atoms because of high energy and different charges [11] [12].

Moreover, cosmic radiation released high energy (>1 MeV) which can trigger the soft errors in semiconductor devices through the production of secondary ions by the silicon nuclei with the silicon nuclei [11]. Complex cascade of secondary particles can be produce by mixing the reaction of the Earth's atmosphere with galactic origin of the cosmic rays [11]. Hence, greater energy from the cosmic radiation has verified to be the main factors of soft errors in DRAM devices in the mid-1990s [14]. In electronic devices ,the third soft error mechanism of ionizing particles is the secondary radiation from the interaction of cosmic ray between boron and neutrons [11].

The formation of radiation by low-energy cosmic neutron involved the interaction with isotope boron-10 (^{10}B is commonly used as p-type dopant for junction formation in