DESIGNING 8-BIT MULTIPLIER

YEE MING FATT

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To my beloved Family & Friends

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ABSTRAK

Asas Pendaraban bagi dua digit binari merupakan antara operasi yang terpenting di dalam pemproses isyarat digital. Oleh itu, rekeaan blok untuk mendarab adalah amat penting di dalam prospek 'VLSI' terutamanya apabila kelajuan dan kawasan merupakan faktor utama dalam rekaan. Walaupun pelbagai jenis rekaan untuk blok pendarab telah diusulkan beberapa tahun kebelakangan ini, setiap satunya mempunyai kelebihan dan kelemahannya yang tersendiri.

Rekaan blok pendarab yang baru yang berdasarakan rekaan blok pendarab tradisional telah diperkenalkan dalam tesis ini. Pada masa yang sama, beberapa cara rekaan yang bermutu untuk asas blok juga diaplikasikan dalam rekaan pendarab ini, contohnya mengunakan blok penambahan lihat kehadapan aras dua yang pantas dan cuma memerlukan ruang yang kecil dalam fabrikasi. Keputusan eksperimen untuk blok pendarab ini (dari '*CAD*') telah dibandingkan dengan blok pendarab tradisional dari keupayaan pemprosessan.

ABSTRACT

The Fundamental of Multiplying two binary Numbers is the most often use arithmetic operation in the Digital Signal Processor. Therefore, Multiplier design block is especially crucial in VLSI prospectus when Speed and Area is the concern. Many of the Design Topologies Regarding this operation has been approached over the years. However, each of this has its own Advantage as well as drawbacks.

Based on the Conventional Building block, the new approach of Multiplier is introduced in this thesis. Several comprehensive and qualitative of basic structure are also contribute in this design in order to ease the performance of operation. For example, two's level Carry Lookahead Adding block which is optimize in speed and space economy is applied in the adding process. The design performance has then evaluated comparatively to conventional Multiplier based on the resulted value from the Simulation that has been carried out in the appropriate CAD environment.

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ACRONYMS

Altera	Altera Corp
ALU	Arithmetic Logic Unit
ASIC	Application Specific Integrated Circuit
CAD	Computer Aided Design
CLA	Carry Lookahead Adder
CMOS	Complementary Metal Oxide Semiconductor
CPLD	Complex Programmable Logic Device
DUT	Device Under Test
FET	Field Effect Transistor
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
GND	Ground
HDL	Hardware Description Language
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type MOSFET
NRC	Non Recurring Cost
OrCAD	OrCAD System Corp
PDN	Pull Down Network
PDP	Power Delay Product

PLD	Programmable Logic Device
PMOS	P-type MOSFET
PUN	Pull Up Network
RTL	Register Transfer Level
SIA	Semiconductor Industry Association
SPLD	Sequential (Simple) Programmable Logic Devices
tpd	Time Propagation Delay
VHDL(VHSICHDL)	Very High Speed Integration Circuit HDL
VLSI	Very Large Scale Integration

CHAPTER 1

INTRODUCTION

1.1 Digital Era

Digital science has become a dominant technology in the electronic arena. The dramatically advancement of this technology during the past three decades resulting from the development of various technology has absolutely easing the almost all areas of human life. Recently, one commonly use of metric has shown that a single complex logic chip has now contains more than a million (10^6) or so switching devices with the number of transistor exceeded 100 million (10^8). These figures also reflect that the increasing in size of logic design has become another critical challenge in fabrication of dense electronic integrated circuit.

Very Large Scale Integration technology or its acronyms VLSI is a major solution force arises after this matter. This age remarkable technology has made possible to translating the huge size of circuit that may be very intricate and extremely economical in space specification to a small piece of single submicron dimension silicon subtract yet optimizing the speed and power requirements.

However, the high cost of chips fabrication is the major drawbacks of conventional VLSI process, this panorama has become the foremost interesting in VLSI discipline and thus has yield the advent of several new fashions of chip

designing technologies over the years, this includes of renowned Programmable Logic Device (PLD) technology that offer the low cost solution as well as flexibility in chip designing process.

1.2 Project Description

The heart of every digital signal processing Integrated Circuit (IC) is its data path. Which, this can be also defined as the data manipulation and derivation platform. Data Path is especially crucial circuit component when area, power dissipation and speed are into concern. Most of the data path of digital processing IC is constructed by the arithmetic units such as Adder, Substractor, divider and finally the basic operation that found in the most arithmetic components, Multiplier.

This project attention is to design a new approach of Multiplier in terms of speed optimization as well as analysis towards its testability features that can potentially influence the performance.

To ensure the optimization level of multiplier, the fundamental logic network circuits were prior studied extensively and developed by using suitable design entry, this will also become a basic component later in Multiplier design. Furthermore, the design in this report has been implemented both in Transistor level view and VHDL that simulated and synthesized in proper Computer Aided Design (CAD) tools. Last but not least the extended resultant output from multiplier will then be analyzed carefully and documented.

1.3 Project Objective

The goal of this project is to design an alternative multiplier that optimize in term of speed as well as the potential in layout designing comparatively with conventional Array Multiplier design. This particular project also is by means to address the important prospect of VLSI design such as transistor integration circuits design technology that use to construct Multiplier.

1.4 Thesis Outlines

After the short introduction regarding the digital technologies trend, this chapter will project the highlight to the project description and project objective respectively.

Chapter 2 introduces the philosophy and property of MOSFET that covering the description of principles and structure of general circuit design, this including Inverter, Half Adder, Full Adder, and fundamental of multiplier operation. For more, the chapter also dedicated to the understanding of CAD design tools and its related terms. The strategy to develop a multiplier circuit and algorithm design will be thoroughly described in ***Chapter 3***.

Chapter 4 presenting the bottom-up simulation result that yield by the design in preceding chapter as well as the analysis towards its performance issue and algorithm proficiency while conclusion with the recommendation are emphasized in ***Chapter 5***.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

As mentioned in the first chapter, the integration density and performance of Integrated Circuits (IC) have gone through an astounding revolution in the recent two decades. In the 1960s, Cordon Moore, then with Fairchild Corporation and later cofounder of Intel has predicted that the number of transistor that can be integrated on a single die would grow exponentially with time. This prediction and later called as Moore's law has proven to be amazingly prophet [Moore65] [12].

The trend of technology in materials, fabrication as well as design process has shown the maturity in this discipline. Many integrated circuits in the market today have embedded with a very large number of transistors either for functional or performance purposes, this is therefore, significant to classify the IC itself upon its feature size. Table 2.1 shows the Semiconductor Industry Association (SIA) roadmap and the Classification of IC by device count proportional to the increasing of the number of transistor per chip [14].

	Year					
	1999	2001	2003	2006	2009	2012
Transistor Gate Length (μm)	0.14	0.12	0.10	0.07	0.05	0.035
Transistor Per Chips (cm^2)	14 Millions	16 Millions	24 Millions	40 Millions	64 Millions	100 Millions
Chip Size (mm^2)	800	850	900	1000	1100	1300

Table 2.1: SIA Roadmap (Classification IC by Device Count)

However, some other factor also have to be carefully taking into concern during the design of the complex IC, this including, Power, Speed, Cost and Area, where, normally this will directly influencing effect of the product itself of the market and end user.

Conventional design with manual component integration method with using breadboard level is then has proved impractical for designing integrated circuit due to poor design productivity, fixed function, long design cycle time and high cost associated with ICs fabrication. Therefore, some other solution has been introduced to resolve this particular problem such As Sequential (or simple) Programmable Logic Devices (SPLD), Complex Programmable Logic Device (CPLD) and Field Programmable Gate Array (FPGA). Each of these devices normally comes with a set of CAD tools which are dynamic and powerful that provide the necessary software to facilitate the hardware fabrication of the unit [8] [6].

This chapter mainly concentrates to the fundamental and functional theory of various types of logic gates as well as introduction to Programmable Logic Device flow and its respective issues.

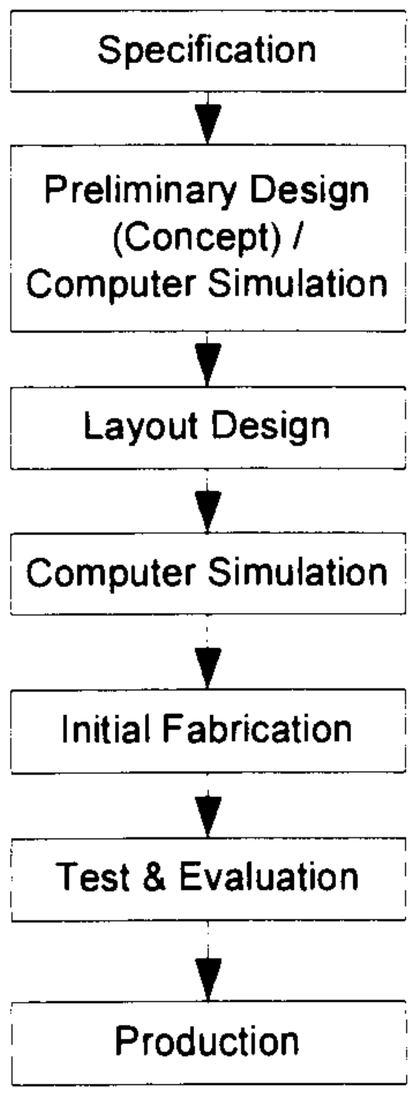

Figure 2.1: Simplify block diagram of conventional IC design process [6].

2.2 MOSFET Architecture and Philosophy

Metal Oxide Semiconductor or known as MOS is a most commonly used Field Effect Transistor in both analog and digital circuit in today market. The principle usage of this particular device are to direct controlling of logic signal (Switching application) in high-density digital VLSI IC design. Its name of MOS has directly portrayed the layering integration of three different materials these are, Metal, Oxide and Semiconductor (usually Silicon but some also use mixture of silicon and germanium SiGe) in sequence [29].

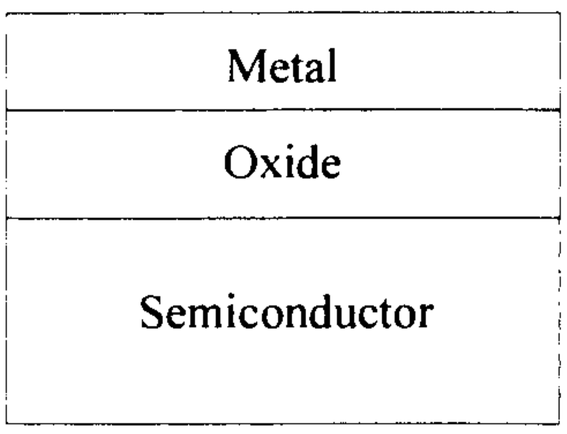

Figure 2.2: Basic MOS composition

The MOS behavior of charge carriers in semiconductor is controlled by electric fields in the structure that normally established by externally applied voltages. This is then however has allows for the construction of MOSFETs (MOS field effect transistor) [11].

2.2.1 NMOS and PMOS

MOSFETs offer two types of transistors, n-Channel MOSFET and p-Channel MOSFET and are accordingly called an NMOS or PMOS, which fabricated as individually packaged discrete components for high power applications as well as by the hundreds of millions inside an IC [28].

As far as NMOS is concern, this device is a passive device that fabricated on a p-type substrate. A single crystal silicon wafer that provide a physical support of the device, two heavily doped n-typed regions, a thin layer of silicon dioxide (SiO_2) of thickness of $(2\text{-}50nm)^2$ [1] that performed as insulator to prevent the charge lost by carrier through the gate. Metal is deposited on top of the oxide layer to form gate electrode of the device this also made the source region, gate