UNIVERSITI MALAYSIA SARAWAK
UNIMAS

Faculty of Engineering

MEASURING CURRENT LEAKAGE IN CMOS

Nuraisyah Binti Siddek

Bachelor of Engineering with Honours
(Electronics and Computer Engineering)
2006

UNIVERSITI MALAYSIA SARAWAK

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BORANG PENYERAHAN STATUS TESIS

Judul: **MEASURING CURRENT LEAKAGE IN CMOS**

SESI PENGAJIAN: **2005/2006**

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MEASURING CURRENT LEAKAGE IN CMOS

NURAISYAH BINTI SIDDEK

This project is submitted in partial fulfillment of
the requirements for the Degree of Bachelor of Engineering with Honors
(Electronics and Computer Engineering)

Faculty of Engineering
UNIVERSITI MALAYSIA SARAWAK
2006

To my parents, **Haji Siddek bin Haji Jamiruddin and Hajah Mardianah binti Shahrun**, my beloved siblings, and friends for their greatest love and their fully support of my study and work.
To my supervisors and all lecturers for their guidance and unlimited support and sacrifices they have made.

ACKNOWLEDGEMENT

Bismillahirrahmanirrahim

"In the name of Allah most gracious and most merciful"

It is time to write my gratitude to all the people who helped me finish the once considered impossible project, I become incompetent to choose the exact words to express my heartily thanks to them. I am afraid what I could do here is to just list them out now and bear in my heart all the appreciation to them forever.

I dedicate a special gratitude to **Mr. Norhuzaimin Julai** and **Mdm. Siti Kudnie Sahari**, this work is impossible to complete without your guidance, distinctive ideas, and scrutiny. I always appreciate your kindness for bearing with my fallacy and guide me through completing this project.

Special thanks to all lecturers and lab technicians for their tremendous moral support. To my parents **Haji Siddek bin Haji Jamiruddin** and **Hajah Madianah binti Shahrun**, my siblings; **Noraini, Nasir, Norainah, Nazir, Norazarinah, Najib** and **Nazim** who provide financial, greatest love and fully support, thanks you very much for believing in me. I would like to extend the appreciation to **Along, Angah, Oyen, Ann, Aina, Nuri, Jard** and fellow course mates for their endless support.

Finally yet importantly, I would like to thank the staff of Engineering Faculty, University Malaysia Sarawak for facilitating me to complete this project successfully.

ABSTRAK

Dalam era teknologi yang serba canggih, kebanyakan peralatan yang digunakan disekeliling kita adalah berasaskan CMOS yang mengandungi bukan sahaja beribu malah berjuta-juta transistor dimuatkan dalam satu chip. Justeru, untuk mencapai persembahan dan kemampuan perlatan yang tinggi, sejajar dengan penggunaan kuasa yang rendah, beberapa item perlu dikurangkan setiap tahun, contohnya, dimensi peralatan dan voltan yang dibekalkan. Malangnya, pengurangan ini menyebabkan meningkatnya kebocoran arus yang akan memberi kesan yang sangat besar terhadap penggunaan kuasa. Objektif utama projek ini adalah untuk mengukur kebocoran arus dalam peralatan CMOS dengan menggunakan software yang sesuai. Masalah utama bagi projek ini adalah untuk menentukan saiz transistor yang paling optima dengan menguji panjang dan lebar transistor agar menghasilkan kebocoran arus yang paling kecil. Justeru, bagi menyelesaikan masalah tersebut, 'Microwind Simulation Software' adalah kaedah yang dicadangkan untuk mengukur kebocoran tersebut. Projek ini akan memberikan pengetahuan yang mencukupi tentang factor-faktor yang menyebabkan kebocoran arus dan jenis-jenisnya. Di samping itu, projek ini juga akan menentukan gate optima dalam menghasilkan kebocoran arus yang paling rendah. Perbandingan antara rekabentuk yang mengaplikasikan litar yang mempunyai kebocoran arus rendah dengan litar biasa akan dikaji.

ABSTRACT

In the sophisticated of technology era, almost all of devices around us are based on CMOS that consist of not only thousand but also million transistors only in one chip. Therefore, to achieve higher performance and reliability of CMOS devices, along with low power consumption, a few items should be reduced over the years such as device dimension and supply voltage. Unfortunately, these reductions have also caused in increase leakage current that can severely affect power consumption in a circuit. The main objective of this project is to measure the current leakage in CMOS devices using appropriate software. Generally, the major outcome of this project is to determine the optimum transistor sizing by analyzing the width and length of transistor so that it will produce very small current leakage. Therefore, in order to overcome that problem, Microwind Simulation Software is a method that suggested measuring the current leakage. This project will provide sufficient knowledge on factors that contribute to current leakage and its mechanisms. In addition, the optimal gate that produces the smallest current leakage will be explained thoroughly. Finally yet importantly, comparison between designs that applied the smallest current leakage and common circuit are concluded.

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LIST OF ABBREVIATIONS

BTBT	- Band-to-Band Tunneling
CAIS	- Center for Academic and Information Service, UNIMAS
CMOS	- Complementary MOSFET
DIBL	- Drain-induced barrier lowering
DRC	- Design Rule Checker
GIDL	- Gate induced drain leakage
IG	- Gate direct-tunneling leakage
ISUB	- Subthreshold (weak inversion) leakage
IREV	- Reverse-biased junction leakage current
L	- Channel length
MOSFET	- Metal Oxide Semiconductor Field-Effect Transistor
NMOS	- n-type MOSFET
PMOS	- p-type MOSFET
W	- Transistor width

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CHAPTER 1

INTRODUCTION

1.1 Background

Aggressive scaling of CMOS devices in each technology generation has resulted in higher integration density and performance. Simultaneously, supply voltage scaling has reduced the switching energy per devices. However, the leakage current that can be defined as the current flowing through the device in its 'off' state has increased drastically with technology scaling [9]. Reports indicate that 40% or even higher percentage of the total power consumption is due to the leakage of transistors. This percentage will increase with technology scaling unless effective techniques are introduced to bring leakage under control.[8] Hence, the estimation of the total leakage is absolutely necessary for designing low power logic circuits. Basically, there are six mechanisms of current leakage that has been recognized.[2] However in reality, among different leakage mechanisms in scaled devices, only three major that mostly contribute to total leakage current which are identified as subthreshold leakage, gate leakage and junction leakage.[9]

The threshold voltage scaling and its reduction due to Short Channel Effects, result in an exponential increase the subthreshold current.[9][7] The oxide thickness scaling, required to maintain reasonable Short Channel Effects immunity, results in a considerable direct tunneling current through the gate insulator of the transistor. In scaled devices, the higher substrate doping density, and the application of the 'halo' profiles that is used to reduce Short Channel Effects cause significantly large Band-to-Band Tunneling (BTBT) current through the reverse biased drain-substrate and source-substrate junctions. In the small devices each of different leakage components increases resulting in a dramatic increase of the overall leakage.[9]

The magnitudes of each of these components depend strongly on the device geometry namely, channel length, oxide thickness and transistor width.[9] Different leakage current components in the devices vary differently with varying temperature. Subthreshold and junction leakage show a strong dependence of temperature, whereas gate leakage is relatively insensitive to temperature variations.

1.2 Objectives

In this project, a few methods on how to measure current leakage in CMOS will be studied. Basically, focus will be on qualitative method which is using simulation software such as MicroWind to observe and analyze variation occurred in current leakage. Some of the objectives of this project are:

i) To study and analyze the characteristic, factors and mechanism of current leakage in CMOS

ii) To gain some knowledge and experience on how to use simulation software such as MicroWind in order to construct the CMOS design and analyze the output obtained.

iii) Analyze the optimal current leakage among different parameter of transistor sizing

iv) Choose the basic gate that produce the optimal current leakage

v) Compare the current leakage of common CMOS design with the new design of gate that produces the optimal current leakage.

1.3 Scope and Study

This final year project is covered and concentrated on:

i) Measuring current leakage in CMOS - using MicroWind circuit simulation software

ii) Previous studies and research on how to compute and analyze current leakage in order to reduce power consumption in CMOS devices.

iii) Observe change that occurred in current leakage when applying various values of a few parameters such as transistor weight (W), and channel length (L).

It is hoped that this study will provide more information and knowledge on how to measure and analyze current leakage occurred in CMOS devices and can be useful as a reference in the future research.

1.4 Project Organization

This project is focused on how to measure the current leakage in CMOS. Throughout this task, discussion on the mechanisms of current leakage and its design technique are made based on the findings that are acquired from journal, books and researches by others. Then analysis on current leakage is done by using simulation software to figure out the optimal value of parameters in order to obtain the minimum current leakage. Also comparison between qualitative and quantitative results of current leakage will be discussed.

Chapter 2 is the Literature Review section. The basic theoretical understanding on the mechanisms and factors of current leakage are represented in this section. However, the research will be focused on gate induced drain leakage, junction leakage and subthreshold leakage only. Since, these three components are contribute more in total current leakage, the rest components such as punchthrough, hot carrier injection and gate oxide tunneling leakage can be neglected. The review on the design techniques of this static CMOS circuit for current leakage is consist of Gate Leakage Current in a Single Transistor, Structure Dependence, and State Dependence. In this section also, the current leakage calculation will be introduced.

In Chapter 3, the methodology for the case study will be presented. It can be classified into two methods, which are quantitative and qualitative method. Besides that in this section, basic flow of the overall activity in this project also enclosed for better understanding. This flow chart described how the project is carried on beginning from the information and facts collection, circuit designing, simulating, calculating, and analyzing the output to observe the current leakage improvement.

Chapter 4 will be devoted to the result and discussion section. Analysis on current leakage measurement will be done on the graph obtained through their equation and simulation process. Next discussion on the enhancement of the current leakage will be made.

Chapter 5 will be the conclusion and recommendation section where the whole activities on the project are concluded and suggestions are made for future works.