POWER OPTIMIZATION OF LOW NOISE AMPLIFIER

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Bachelor of Engineering (Hons) in Electronics (Telecommunications)
2014
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POWER OPTIMIZATION OF LOW NOISE AMPLIFIER

ABDUL HAAFIDZ BIN RAMLI

Thesis is submitted to
Faculty of Engineering, Universiti Malaysia Sarawak
in partial fulfilment of the requirements
for the degree of Bachelor of Engineering (Hons) in
Electronics (Telecommunication)
2013/2014
TO MY BELOVED FAMILY, FRIENDS AND MY LOVE
ACKNOWLEDGEMENT

Alhamdulillah, thanks to Almighty ALLAH S.W.T. for giving me a chance to complete this project. All the good encouragement, devotions, and prayers are due to ALLAH whose blessing and guidance have helped me throughout the entire project.

I would like to thank my project supervisor, Mdm. Dayang Nur Salmi Dhamizah binti Awang Salleh, for her knowledgeable guidance and support which leads to the complete success of this project. I appreciate all the valuable time she spent on the progress of the project on weekly basis until the final completion.

My thanks also go to my beloved family and friends who provide invaluable morale supports and advices, especially during hard times of the project development. I would like to thank them for their caring understanding and patience throughout the project development duration.
ABSTRACT

Low noise amplifiers are widely used in wireless communications. LNA can be found in almost all RF and microwave receivers in both commercial and military applications such as cellular phones, WLANs, Doppler radars and signal interceptors. This paper describes power optimized CMOS low noise amplifier (LNA) intended for Bluetooth application. Employing CMOS inverter as a core of the proposed LNA, the extra gain is obtained by adding a second stage gain control mechanism which is to control the gain. A comprehensive method to optimize CMOS Inverter Current Reused (CICR) family is attained and with gain control mechanism implementation to achieve low noise and high 1dB compression point simultaneously without increasing any circuit and power consumption. The designed LNA is based on 0.18μm CMOS technology and overall performance using simulation environment is presented in this paper.
ABSTRAK

Penguat hingga rendah digunakan secara meluas dalam sector komunikasi tanpa wayar. Ia digunakan dalam hampir semua penerima frekuensi radio dan gelombang mikro samada keperluan mahupun komersial. Contohnya, telefon bimbit, WLANs, Radar Doppler dan pemintas isyarat. Kertas kerja ini membentangkan peningkatan kuasa penguat hingga rendah CMOS yang disesuaikan untuk aplikasi Bluetooth. Penyebab CMOS digunakan sebagai teras kepada penguat hingga rendah yang dicadangkan. Lebih gandaan voltan telah diperolehi dengan menambah kekerapan kedua dalam mekanisme kawalan gandaan voltan yang berfungsi untuk mengawal gandaan voltan. Kedua yang menyeluruh dilakukan untuk pengoptimuman penyelenggaraan penggunaan semula arus penguat hingga rendah (CICR) telah dicapai. Pelaksanaan mekanisme kawalan gandaan voltan untuk mencapai hingga rendah dan mampu 1dB yang tinggi pada masa yang sama tanpa meningkatkan penggunaan kuasa. Reka bentuk penguat hingga rendah ini berpandangan kepada 0.18µm teknologi CMOS dan prestasi keseluruhan dengan menggunakan suasana simulasi dibentangkan dalam kertas kerja ini.
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CHAPTER 1

INTRODUCTION

1.1 Introduction to Low Noise Amplifier

Low noise amplifiers are widely used in wireless communications. Almost all RF and microwave receivers in both commercial and military applications such as cellular phones, WLANs, Doppler radars and signal interceptors use LNAs. Depending upon the system in which they are used, LNAs can adopt many design topologies and structures. In commercial applications LNAs aim toward high integration, and low voltage and bias currents. LNAs are usually placed at the front end of a receiver system, immediately following the antenna. The purpose of the LNA is to boost the desired signal power while adding as little noise and distortion as possible [1].

![Diagram of LNA topology](image)

Figure 1.1 Basic topology of LNA [1]
General considerations of LNA design is governed by several parameters. They are noise figure, gain, input return loss, stability, linearity, bandwidth, and power dissipation. It is well known that the first amplification stage dominates the total NF of the system and thus the noise optimization of this first stage is important [2].

1.1.1 Noise Figure

The noise figure of the LNA directly adds to that of the receiver. Typical noise figure is at 6 to 8 dB, LNA having about 2 to 3 dB, antenna switch of duplexer at 0.5 to 1.5 dB and remaining chain about 2.5 to 3.5 dB. While these values provide a good starting point in the receiver design, the exact partitioning of the noise is flexible and depends on the performance of each stage in the chain.

1.1.2 Gain

The gain of the LNA must be large enough to minimize the noise contribution of later stages.

1.1.3 Input Return Loss

The input return loss can be expressed as the quality of the input match, defined as the reflected power divided by the incident power. Input matching between the antenna/LNA could improve the overall performance. Poor matching at the input cause voltage attenuation, uncharacterized loss, and significant reflections.

1.1.4 Stability

In the situation the user of a cell phone wraps his/her finger around the antenna, the antenna impedance changes. For all source impedances at all frequencies, the LNA must remain stable.
1.1.5 Linearity

In most application, the LNA does not limit the linearity of the receiver. Thus, LNA design and optimization are done with little concern for the linearity.

1.1.6 Bandwidth

The LNA -3 dB bandwidth must be substantially larger than the actual band so that the roll-off at the edges remains below 1 dB.

1.1.7 Power dissipation

In most receiver designs, circuit's power dissipation is less focused compared to the noise figure.

1.2 CMOS and Power Optimization of Low Noise Amplifier

A proportional downscaling of the supply voltage is required to maintain the device reliability. At the same time, a relatively large threshold voltage (V_t) needs to be maintained to limit the OFF current in transistors, as shown in Figure 1.2 [3].

![Figure 1.2](image)

Figure 1.2 Supply and threshold voltage scaling over time as line widths decrease [3]
Portability and reliability are important in low power circuit design. It is due to the use of portable electronic devices mainly laptop and mobile phones. The need for greater portability and reliability affects the limitation on battery weight and size, inducing severe constraint on system power dissipation.

Up until recently, there has been considerable interest in the use of CMOS low-noise amplifiers (LNA) for RF and wireless systems, especially frequency modulation (FM) radio receivers. Such a radio receiver can be used as an expansion of a variety of portable audio devices such that the devices can offer FM radio reception. For RF integrated Circuits (RFIC) operating at FM frequency bands (centered around 100 MHz), an on-chip inductor is rarely used for the LNAs [4].

Driven by the insatiable demands for lower costs and higher bandwidth, technology is moving towards higher integration while operating at lower supply voltages. As process geometries decrease, operating voltages must be scaled down due to the increased electric fields and reduced breakdown voltages caused by higher doping profiles. This decrease is suitable for low power consumption devices. However, the threshold voltage ($V_{th}$) of a MOS transistor decreases at a much lower rate than the supply voltage with the decreasing CMOS process. This limitation makes the RFICs design more difficult, hence new topologies are needed to face the complexity due to the lowered supply voltage and improve the overall performances [5].
From the figure below, it is observed that scaled down device yields wider range of threshold voltage ($V_{th}$).

![Graph showing gate length and voltage threshold trends](image)

Figure 1.3 Gate length and voltage threshold trends [6]

Furthermore, low-cost and compactness, low power consumption, high linearity in the pass band, and acceptable stability increase its practical importance. In order to enhance the quality of front end amplifiers’ operation, they should be considered as a whole rather than a single block; i.e., all the elements included in the structure must be studied, designed, and optimized simultaneously. Techniques are developed to optimize power in LNAs. Among the published optimization techniques are mostly applied to either common source (CS) or cascade LNAs [7].

Typical applications of 2.4GHz, such as Bluetooth, promise mass market development with high volume production. Wireless control and communication between a mobile phone and a headset, or another Bluetooth component is few of the applications of available in the market.
1.3  Objectives

The objectives determined for this project are as shown below:

- Develop and implement design techniques to achieve power optimization of LNA
- Design CMOS LNA for Bluetooth application

1.4  Report Outline

Chapter 1 is an introduction to the project including the basic of low noise amplifier, the significance of power optimization, and objectives and overall development.

Chapter 2 provides an overview research associated to the project. Reviews based on the power optimization are conducted and theories are reviewed. Related techniques are reviewed and understanding on the most preferred technique is determined. Comparisons on different technique are conducted.

Chapter 3 describes the methodology developed by chosen techniques used to design the LNA. Two stage design of the LNA is developed. Each design is studied carefully to achieve the specification performance of the LNA. Procedures for obtaining the overall performance are added by using the Virtuoso Analog Environment simulation.

Chapter 4 contains the simulation results acquired from the techniques used to design the LNA. Detail analyses are discussed based on the simulation output reading under the Virtuoso Analog Environment simulation.

Chapter 5 is the conclusion of the report. Recommendations are presented in this chapter for resolving the constraints encountered during the project.
CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, comparisons of low noise amplifier (LNA) topologies are conducted to identify the technique used for power optimization application. It is suggested from the preliminary studies that the gain, noise figure and input matching is the main concern in LNA design. These topologies, which are common gate (CG), CMOS inverter current reused (CICR), single stage cascade, and digital gain control are techniques that have been used for power optimization application.

2.2 Differential Common Gate (CG) Active Boost Low Noise Amplifier (LNA)

In 2011, Francois Belmas, Frederic Hameau, Jean-Michel Fournier proposed an inductorless low power (LP) low noise amplifier (LNA) based on the common gate (CG) topology. Gain boosting techniques is combined to enable high gain LP LNA.

The proposed circuit composed of a “main” amplifier (NMOS M1-R, R1) and a so-called “gm-boost” amplifier (NMOS M3-R, R3). There are 3 reasons for the use of CG topology. First, CG circuits are known to be more linear [8]. Secondly, auxiliary CG circuits helps in lowering the input impedance. Thirdly, with $C_{C2}$ when cross coupling technique (CCCT) is applied, it boosts the gm-boost amplifier without extra $P_{DC}$. $R_f$ is defined as the output load of the gm-boost amplifier and by using
current sources $M_{5A, B}$, excessive voltage drop is avoided. The gain bandwidth is enhanced with neutralization capacitors ($C_{C4}$) that cancel the gate-to-drain capacitance of $M_1$ and creates a peaking effect on the $g_{m}$-boost gain.

![Circuit Diagram](image)

Figure 2.1 Schematic of differential CG active boost LNA [9]

### 2.2.1 Input matching technique and gain boost

In most applications, most inductorless LNA circuits with the input 50Ω impedance are either based on shunt-feedback (SFB) structure or common gate (CG) topology [10]. It is noted that high voltage gain, good input matching with low power consumption are required. SFB is built with a pure resistive feedback, where input admittance $G_{IN}$ is the ratio of the voltage gain $A_V$ and resistive feedback $R_F$.

For Figure 2.2(a), $R_F$ does consume power but degrades the output impedance and, thus, the gain capability when $g_{m}$ is small. Alternatively, using a source follower along with $R_F$ is conducted in Figure 2.2(b) but the extra $P_{DC}$ required for $g_{m2}$ limits the performance of the amplifier. Lastly, using common gate
(CG) circuits as in Figure 2.2(c) enable both higher gain and lower input impedance when $g_{m1}$ increases but the condition of input matching forces $g_{m1}$ to be equal to $1/50\Omega=20\mu S$ thus making it not suitable for input matching at low $P_{DC}$.

Figure 2.2  Comparison of (a) Resistive SFB, (b) Active SFB, (c) Common Gate

Figure 2.3 illustrate $g_{m}$ enhancement technique that is applied to increase the gain. The $P_{DC}$-$g_{m}$ tradeoff in common gate (CG) amplifier is avoided. Applying a cross coupling techniques (CCCT), the AC amplifier current is doubled. This technique is known as gate voltage booster by enabling a $g_{m}$-boost effect since the equivalent $g_{m}$ is doubled for constant biasing current [11].

Figure 2.3  Techniques (a) Differential CG amplifier, (b) Differential CG amplifier with CCCT, (c) Principle of $g_{m}$-boost in CG amplifier
2.2.2 Design Parameter

2.2.2.1 Input Matching and Gain

The equivalent voltage gain \( G_V \) and input admittance \( G_{IN} \) are:

\[
G_V = g_m R_1 (1 + 2 g_m R_2) \quad (2.1)
\]

\[
G_{IN} = g_m (1 + 2 g_m R_1) + 2 g_m \quad (2.2)
\]

These values are affected by the loading conditions of the LNA. The 50\( \Omega \) load capacitor strongly affects the final bandwidth. \( R_f \) and \( R_J \) need to be high to provide high gain and low noise and 2.45GHz gain cut-off frequency is acquired. Hence, \( C_{C4} \) is chosen to make the LNA stable. As shown in the Figure 2.4, high capacitance value does not affect the bandwidth but increase the high frequency gain roll-off.

![Figure 2.4](image)

Figure 2.4 Effect of neutralizing capacitor \( C_{C4} \) on gain bandwidth and \( H_{IP3} \) [9]

2.2.2.2 Noise Performance

The \( g_m \)-boost amplifier is made of active noisy components. Designing at low bias current, extra noise sources have to be included. From Figure 2.5, the unmatched
The noise factor of full CGAB LNA is calculated. The main reason of using CCCT on $g_{m, boost}$ is to reduce the noise contributors by half, without the $P_{DC}$ penalty.

\[ F = 1 + F_{M3} + F_{R3} + F_{M1} + F_{R1} \]  \hspace{1cm} (2.3)

\[ F \approx 1 + \frac{(\gamma_{m3})^2}{2\gamma_{m3}R_S} + \frac{1}{2\gamma_{m3}R_S R_X} + \frac{2\gamma_{m1}^2}{\gamma_{m1}R_S(1+\beta_3)^2} + \frac{2(1+\beta_{m3}R_S+\beta_{m1}R_S(\frac{A_1}{\alpha}))^2}{\gamma_{m1}^2R_4R_5(A_1)^2} \]  \hspace{1cm} (2.4)

\[ I_{M1} + I_{M2} = C'sic. \]

**Figure 2.5** Equivalent circuits for noise calculation (2.3 and 2.4) \([9]\)

**Figure 2.6** Simulated and calculated NF vs $g_{m3}$, as $I_{M1}$ decreases, $I_{M2}$ increases \([9]\)