Performance of CMOS Schmitt Trigger

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Abstract

This paper presents the effect of load capacitance and source voltage on performance of proposed Schmitt trigger circuit. The proposed circuit was designed based on Conventional Schmitt Trigger by manipulating the arrangement of transistors and the width-length ratio. All simulation results have been carried out based on Microwind software on three different designs in term of propagation delay, Energy-delay Product and hystheresis. From the result, the proposed full swing CMOS Schmitt Trigger was able to operate as low voltage (0.8V-1.5V).

I. INTRODUCTION

The Schmitt trigger circuit is widely used in analog and digital circuit as wave shaping circuit to solve the noise problem. Beside that this circuit is widely design in various styles in order to drive the load with fast switching, low power dissipation and low-supply voltage, especially for the high capacitive load problem [1].

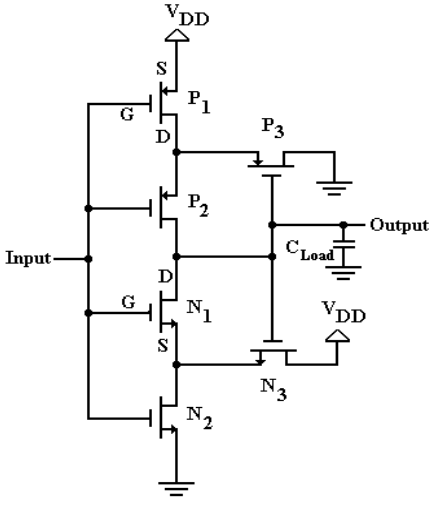

Figure 1. The Conventional Schmitt Trigger

Conventional Schmitt Trigger is shown in Figure 1 and the detail design is presented in [2] where the switching thresholds are dependent on the ratio of NMOS and PMOS. However, this circuit will exhibit racing phenomena after the transition starts. Therefore in this paper, we proposed CMOS Schmitt Trigger circuit which is capable to operate in low voltages (0.8V-1.5V) at high capacitance, less propagation delay and stable hysteresis width.

II. CIRCUIT DESCRIPTION

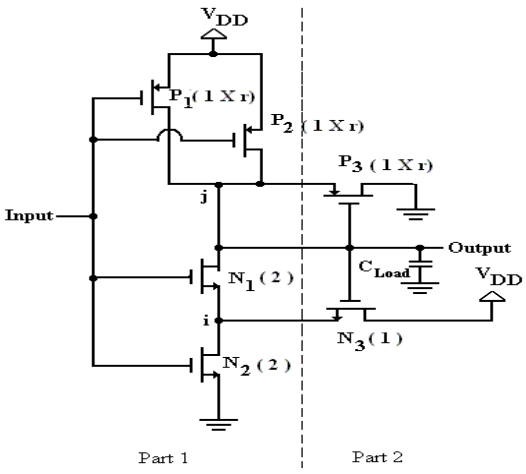

Figure 2. The Proposed Schmitt Trigger

The proposed Schmitt Trigger [3] is shown in Figure 2 and is categorized into two parts which is Part 1 and Part 2. Similarly to Conventional Schmitt Trigger, the proposed circuit is formed by a combination of two sub-circuits, P sub-circuit (which consist of P_1, P_2 and P_3) and N sub-circuit (which consist of N_1, N_2 and N_3). There is no direct connection between the source voltage and ground as P sub-circuit is connected to the path between the source voltage and output while the N sub-