

Low Noise Figure 2.4 GHz Down Conversion CMOS Mixer for Wireless Sensor Network Application

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Abstract— This work proposed a low noise figure 2.4 GHz down-conversion CMOS mixer for wireless sensor network (WSN) application using 0.13- μm Silterra technology. The proposed down-conversion mixer converts a high radio frequency (RF) signal from 2.4 GHz to an intermediate frequency (IF) of 100 MHz through the use of a local oscillator (LO) of 2.3 GHz. The proposed mixer employs a double balance Gilbert-cell topology with integrated input matching at the input stage and a low pass filter at the IF stage. The simulation results indicate that the proposed mixer obtains lower noise figure (NF) of 5.21 dB with an input third-order intercept point (IIP3) of 0 dB. Furthermore, the conversion gain (CG) of 8.6 dB is achieved with the power consumption of 1.57 mW at 1.8 V supply voltage.

Keywords—Conversion gain, double-balance, down-conversion, Gilbert-cell, power consumption

I. INTRODUCTION

Wireless sensor network (WSN) is an application with a highly-demanded since the existence of a wireless generation which is often used in communication technology. In general the WSN is a self-organizing network that contains a large number of sensors which is designed for collecting, processing and transmitting data. The WSN usually applied in the different fields such as military affairs, healthcare, environmental science, industrial monitoring and so on. Fig. 1 shows the architecture of WSN that consist of RF transceiver and baseband processor. The RF transceiver has been assembled with low noise amplifier (LNA), power amplifier (PA), mixer, low pass filter (LPF) and voltage control oscillator (VCO) [1].

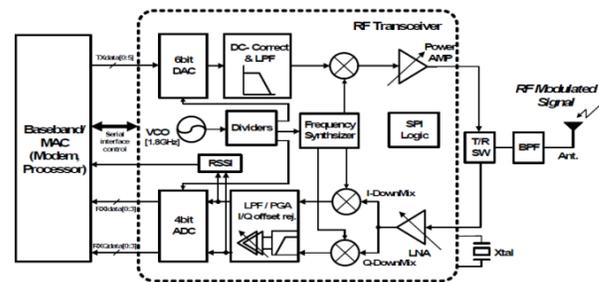


Fig.1. Wireless Sensor Network architecture [1].

Mixer is a most significant circuit block in RF transceiver where it function to transfer the signal frequency to a higher or lower spectrum that generated by the multiplication of two signals [2]. Down-conversion mixer is one type of active mixer that deployed in the WSN architecture which converts a radio frequency (RF) signal that amplified by the LNA into an intermediate frequency (IF) through the multiplication of a local oscillator (LO) signal as depicted in Fig. 2. From the previous work [3-7], there are several important performances parameters that required in designing a low power and high linearity CMOS mixer likes conversion gain, noise figure (NF), mixer linearity such as input 1-dB compression point (P1dB) and input third order intercept point (IIP3), and also power consumption[8].

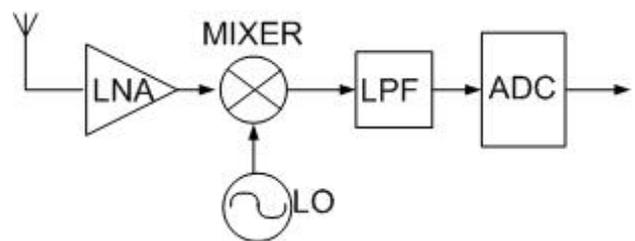


Fig. 2. Down-conversion mixer block diagram.