A 2.4 GHz Two Stage CMOS Class-F Power Amplifier for Wireless Applications

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Abstract. The design of a 2.4-GHz CMOS class-F power amplifier (PA) for wireless applications is presented in this paper. The class- F PA design is implemented using 0.13-µm CMOS process. It utilizes two stages cascade topology and the transistors are arranged in parallel to reduce the transistor's on resistance which correspondingly increase the PA efficiency. The simulation results show that the PA delivers 12 dBm output power and 60% power added efficiency (PAE) into a 50 Ω load. The supply voltage is 1.3 V and the chip layout is 0.66 mm².

Introduction

Recently, a modulation scheme for modern wireless systems such as 4G long term evaluation (LTE) and mobile worldwide interoperability for microwave access (MiMAX) utilize orthogonal frequency division multiplexing (OFDM) which has a high peak-to-average power ratio (PAPR) resulting in degradation of efficiency in transmitters [1]. Therefore, the high efficiency, low cost, compact and high integration power amplifier (PA) becoming an important issue in designing a circuit with relatively high power efficiency.

Over past years, the PA technology has emerged rapidly and has become highly integrated. The circuit design has involved several process technologies such as CMOS, GaN, GaAs and SiGe BiCMOS [2-5]. However, CMOS has become a good technology due to their high integration and low cost. Nevertheless, the main challenge in design PA using CMOS technology is the low breakdown voltage at deep sub-micron and thus limits the maximum drain to gate voltage. Normally, the supply voltage is two times lower than the drain voltage. Thus, the transistor has to work at a low supply results lower power and low efficient.

Generally, PAs are a last part in the transmitter front-end of RF transceivers. The role of a PA is to amplify a signal to a certain level of power which will ensure that the receiver will receive a transmitted signal across some distance. PA can be defined as an electronic amplifier used to convert a low signal power into a large signal power of radio frequency (RF) especially in order to drive the antenna in a transmitter [6]. Good gain, high efficiency, good input and output return loss, high linearity (P1dB) and low heat dissipation is a demanding PA.

This paper describes a two stage class-F PA at 2.4 GHz designed using 0.13-µm CMOS process. The proposed design consists of driver stage, amplifier stage and harmonics filtering to increase power