
**Faculty of Engineering**

# Step-Up Multiple-Input Battery Integrated High-Gain DC-DC Converter for Renewable Energy Application

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**Doctor of Philosophy**
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# Step-Up Multiple-Input Battery Integrated High-Gain DC-DC Converter for Renewable Energy Application

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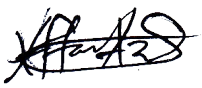
## DECLARATION

I declare that the work in this thesis was carried out in accordance with the regulations of Universiti Malaysia Sarawak. Except where due acknowledgements have been made, the work is that of the author alone. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.



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## ABSTRACT

The challenges faced by renewable energy (RE) sources like solar and wind energy, are a limitation to their potential as viable replacement to fossil fuels in the foreseeable future. Top of these are the problems of irregular or unpredictable availability and low output voltage levels. Multiple input DC-DC converters (MIC) provide the liberty to apply more than one RE source in order to ameliorate the shortcomings. For hybrid RE systems (HRES), it is required that the DC voltage at the inverter level is within the 300 Volts (*V*) to 450 *V* range. This means that MICs should deliver a high voltage gain during operation. In addition, the stochastic nature of RE sources mean that MICs be fitted with battery storage capability to handle periods of power unavailability or abundance. Such HRES should have an optimal energy management profile. In this project, a three-input DC-DC converter has been proposed using the non-coupled inductor and boost technique. The aim of this project is to design a three-input converter that produces a high voltage gain, and possesses bidirectional battery storage and two unidirectional ports. The configuration is developed. Three operation modes are obtained for the three-inductor topology and the respective output voltage equations derived. The proposed topology has been investigated theoretically and simulated via the MATLAB/Simulink platform. Software and hardware integration of a designed prototype has been carried out using dSPACE DS1104 digital controller board to generate switching signals. The prototype converter is able to deliver a measured output voltage of 315 *V* with input voltage of 12 *V* and 24 *V* for two input sources in the primary operation mode. The battery discharging during the second operation mode supported a meagre 1.11 % reduction in output voltage despite decreased input voltage levels from the RE sources. Charging the battery during the third operation mode produced a 4.35 % decrease in output voltage. The energy management algorithm proposed can deliver power via single, double

or triple source depending on load status. The artificial neural network controller adapted for control of the primary operation mode showed good voltage regulation by eliminating overshoots and reducing the settling time by 30 %. The RE sources are able to individually or simultaneously charge the battery while delivering energy to the load. All the input sources are able to deliver power to the load depending on the integrity of supply. Finally, the simulations and experiments conducted show proof of concept for the developed converter.

**Keywords:** Boost, converter, high gain, multiple input, non-coupled inductor, renewable energy

***Pembangunan Penukar DC-DC Tiga Input Bersepadu Bateri untuk Aplikasi Tenaga Boleh Diperbaharui***

## *ABSTRAK*

*Cabaran yang dihadapi oleh sumber tenaga boleh diperbaharui (RE) seperti tenaga suria dan angin, merupakan had kepada potensi mereka sebagai pengganti yang berdaya maju kepada bahan api fosil pada masa hadapan. Antaranya ialah masalah ketersediaan yang tidak teratur atau tidak dapat diramalkan dan tahap voltan keluaran yang rendah. Penukar DC-DC berbilang input (MIC) memberikan kebebasan untuk menggunakan lebih daripada satu sumber RE untuk memperbaiki kelemahan. Untuk sistem RE hibrid (HRES), voltan DC pada aras penyongsang dikehendaki berada dalam julat 300 Volt (V) hingga 450 V. Ini bermakna bahawa MIC harus memberikan keuntungan voltan tinggi semasa operasi. Di samping itu, sifat stokastik sumber TBB bermakna bahawa MIC dipasang dengan keupayaan penyimpanan bateri untuk mengendalikan tempoh ketiadaan kuasa atau kelimpahan. HRES sedemikian harus mempunyai profil pengurusan tenaga yang optimum. Dalam projek ini, penukar DC-DC tiga input telah dicadangkan menggunakan teknik induktor dan rangsangan tidak berganding. Matlamat projek ini adalah untuk mereka bentuk penukar tiga input yang menghasilkan keuntungan voltan tinggi, dan mempunyai storan bateri dua arah dan dua port satu arah. Konfigurasi dibangunkan. Tiga mod operasi diperolehi untuk topologi tiga induktor dan persamaan voltan keluaran masing-masing diperolehi. Topologi yang dicadangkan telah disiasat secara teori dan disimulasikan melalui platform MATLAB/Simulink. Penyepaduan perisian dan perkakasan bagi prototaip yang direka telah dijalankan menggunakan papan pengawal digital dSPACE DS1104 untuk menjana isyarat pensuisan. Penukar prototaip mampu menyampaikan voltan keluaran terukur 315 V dengan voltan input 12 V dan 24 V untuk dua sumber input dalam mod operasi*

*utama. Penyahcasan bateri semasa mod operasi kedua menyokong pengurangan voltan keluaran sebanyak 1.11% walaupun tahap voltan masukan menurun daripada sumber RE. Mengecas bateri semasa mod operasi ketiga menghasilkan penurunan 4.35% dalam voltan keluaran. Algoritma pengurusan tenaga yang dicadangkan boleh menyampaikan kuasa melalui satu, dua atau tiga sumber bergantung pada status beban. Pengawal rangkaian saraf tiruan yang disesuaikan untuk kawalan mod operasi utama menunjukkan peraturan voltan yang baik dengan menghapuskan overshoot dan mengurangkan masa penyelesaian sebanyak 30 %. Sumber RE dapat mengecas bateri secara individu atau serentak sambil menghantar tenaga kepada beban. Semua sumber input mampu menghantar kuasa kepada beban bergantung kepada integriti bekalan. Akhir sekali, simulasi dan eksperimen yang dijalankan menunjukkan bukti konsep untuk penukar yang dibangunkan.*

***Kata kunci:*** *Rangsangan, penukar, keuntungan tinggi, input berbilang, induktor tidak berganding, tenaga boleh diperbaharui*

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| | |
|---|---|
| A | Ampere |
| AC | Alternating Current |
| ANN | Artificial Neural Network |
| BITIHGC | Battery Integrated Three Input High Gain Converter |
| CCM | Continuous Conduction Mode |
| DC | Direct Current |
| DCM | Discontinuous Conduction Mode |
| DIC | Double Input Converter |
| FC | Fuel Cell |
| FCBB | Forward Conducting Bidirectional Blocking |
| HRE | Hybrid Renewable Energy |
| HRES | Hybrid Renewable Energy System |
| LC | Inductor Capacitor |
| LQR | Linear Quadratic Regulator |
| MIC | Multiple Input Converter |
| MIMO | Multiple Input Multiple Output |
| NN | Neural Network |
| NVS | Normalised Voltage Stress |
| OFC | Output Filter Cell |
| PCB | Printed Circuit Board |
| PCSC | Pulsating Current Source Cell |
| PI | Proportional Integral |

| | |
|---|---|
| PID | Proportional Integral Derivative |
| PIV | Peak Inverse Voltage |
| PSC | Pulsating Source Cell |
| PV | Photovoltaic |
| PVSC | Pulsating Voltage Source Cell |
| PWM | Pulse Width Modulation |
| RE | Renewable Energy |
| SC | Switched Capacitor |
| SEPIC | Single Ended Primary Inductor Converter |
| SISO | Single Input Single Output |
| SOC | State Of Charge |
| V | Volt |
| VM | Voltage Multiplier |
| VTR | Voltage Transfer Ratio |
| ZCS | Zero Current Switching |
| ZVS | Zero Voltage Switching |

# CHAPTER 1

# INTRODUCTION

## 1.1 Research Background

Contemporary advancements have resulted in an exponential rise in endeavours aimed at advancing and managing renewable energy (RE) sources. Fossil fuels, which have been the main energy source since the discovery of crude oil and its derivatives are known to cause the pollution of the environment, and global warming (Hosseini, 2022). As fossil fuels are burned, a myriad of dangerous gases is emitted. It has been predicted that a flooding could become more severe as the climate conditions become warmer (Takayama et al., 2023).

Possible avenues for environmental pollution and degradation are not limited to burning fossil fuels for power generation. The emissions from the transportation sector are also inimical to the environment. A survey from the United States of America shows that almost thirty percent of the gases responsible for global warming, are emitted by machinery from the transport sector (Reddy & Natarajan, 2018). These statistics have heightened calls on governments to reduce the use of fossil fuels in the power generation and transportation sectors.

The predicted depletion of fossil fuel reserves within the next century raises questions on the longevity of supply for fossil fuel resources. Shafee and Topal (2009), using a modified *Klass* model predicted that the world's crude oil, coal and gas reserves will be exhausted in 35, 107 and 37 years, respectively.

While the availability of fossil fuels greatly relieves electricity generation, there are remote villages where the electricity grid has yet to be installed. Such rural villages abound in the state of Sarawak, Malaysia. Provision of grid electricity to these remote locations is arduous due to lack of access, scanty distribution, and low population relative to the cost of grid extension (John et al., 2021).

The highlighted dilemma faced by fossil fuels and the accessibility of grid electricity to arduous terrains are the reasons for an upsurge in the advocacy for RE sources as an environmentally friendly solution. Popular RE sources like solar and wind, are freely available and involve lower operation and maintenance costs in addition to providing a cleaner alternative to fossil fuels.

Regrettably, there are undesirable factors that hamper the optimal performance and adoption of these RE sources for power generation. The fundamental issues are that of availability, unpredictability, and reliability (Kanapathi et al., 2022). Irregularity of supply has been observed during operation of these energy sources. For example, the solar panels cannot deliver power at night when there is insufficient irradiance. In a similar manner, wind turbine output parameters at any instant could be affected by wind speed and profile. The output voltage of micro-hydro and hydrokinetic turbines depend on the flow rate of water (Buswig et al., 2020). In addition, the output voltage of many RE sources is low, thus impeding their use in high voltage applications (Cardoso et al., 2020).

Solutions have been proffered to address these described challenges. Concerning the issue of low output voltage, direct current (DC) boost converters can enable the increment of output voltage to desired levels (Kanapathi et al., 2022). The DC-DC boost converter takes in a lower voltage and outputs a higher voltage value. In this way, the voltage can be

stepped up to the inverter voltage level. Irregularity in supply by RE sources has necessitated the implementation of hybrid RE systems (HRES). These HRES combine two or more RE sources and incorporate the energy bank. The merger of more than one or more RE inputs gave illumination to the multiple input DC-DC converter (MIC). In the traditional approach to managing several RE sources at the same time, each RE source has its separate DC-DC boost converter and the respective outputs are tied to a common DC bus. This set up result in a larger, more expensive system with complex communication control (Khosrogorji et al., 2016). The modern MIC used almost the same number of components of a single DC-DC converter to perform the same tasks. Thus, it has the advantage of reduced size, and simple control. Besides, it eliminates the restrictions posed by series or parallel connection of RE sources that exist in the traditional MIC.

## 1.2 Problem Statement

The initial application of multiple RE sources for electricity generation saw the use of separate converters connected in series or parallel connected to a common DC bus. This approach implies increased cost, increased input current ripple and output voltage ripple. There is also the difficulty in control of the converters collectively. This shows the unsuitability of such an approach in managing multiple input sources.

The emergence of two input boost converters using diverse techniques has facilitated the simultaneous delivery of power to the load. In this scenario, the higher output voltage can be achieved by either or both respective input sources. However, in the event of surplus or insufficient power as RE sources are known to deliver, there is no battery source to save the excess power or compensate for the shortfall.

The integration of a battery has been investigated in some multiple input boost converters. The battery charging and discharge function has been studied in the three-input boost converter (Ahrabi et al., 2017). The converter combined a boost topology and a buck-boost topology. Hence it delivers power simultaneously to the load, but the voltage gain is low (Kardan et al., 2017). The switched inductor-based MIC had a high voltage gain, but the output voltage of the converter is pegged to the module with the highest potential (Mahmoodieh & Deihimi, 2019).

Regarding the basic control of single input converters, the single or double feedback loop proportional-integral (PI) or proportional-integral derivative (PID) control is widely applied. The nature of MIC control implies that a mature control like the PI control will face challenges when functioning beyond the linearised operating points (Kapat & Krein, 2020). The sliding mode control is bugged with issues of chattering and high frequency losses (Gorji et al., 2019). In addition, the existence of multiple variables in MICs give rise to coupling of these variables. Decoupling becomes increasingly difficult as the order of the MIC increases (Asl et al., 2022).

While the existing battery integrated boost converters addressed the challenge of charging and discharging the battery, their configurations fall short in delivering high output voltage levels. Since RE sources have low voltage levels, it is crucial to develop and study a topology that delivers a higher voltage gain and can deliver to the load from the input ports at optimal levels. Also, it is necessary to investigate a nonlinear control method as a means to reduce complexities associated with decoupling networks' static operating points. In this project, a battery integrated three-input high voltage gain DC-DC converter (BITIHGC) is propounded.

## 1.3 Research Questions

The following research questions have emanated from the problem statement.

i. What MIC configuration would marginally cater to the challenges faced by RE sources?

ii. How would such an MIC regulate the output voltage while superintending the unpredictable nature of RE sources to ensure optimal switching of the working modes?

iii. How would the functionality of such an MIC be ascertained via computer simulation?

iv. How would the functionality of such an MIC be verified by hardware?

The process of solving these research questions will lead this work to the research objectives listed in the succeeding sub-section.

## 1.4 Research Objectives

The primary aim of this work is to fashion a high voltage step-up battery integrated three-input converter for HRE applications. Two RE sources and a battery storage will be integrated in a topology that produces a high voltage transfer ratio (VTR). The specific objectives of this project are:

i. To evolve the configuration of the proposed BITIHGC and obtain the output voltage and dynamic model for the working modes.

ii. To propound an energy management algorithm and adapt a voltage control method for the proposed BITIHGC.

iii. To simulate the working modes and artificial neural network controller of the proposed BITIHGC.

iv. To experimentally validate the working modes and voltage controller of the proposed BITIHGC.

## 1.5 Scope of the Research

The scope of this thesis is developing a battery integrated three input high gain boost converter. This project evolved from modelling and simulation stage to the hardware and software implementation stage. During modelling and simulation, the converter configuration was identified, and major descriptive equations obtained for the respective operation modes and elements. The hardware and software implementation stage consisted of the design and production of the prototype, development of the switching signals via C code to the DS1104 controller board. The voltage control of the converter will be limited to the basic operation mode in which the battery is bypassed. The controls of the battery charging and discharging operation modes are not within the scope of this project.

## 1.6 Thesis Structure

The thesis comprises five chapters. A summary of the chapters is presented hereafter:

Chapter 2 presents a literature review. It explains basic operation and types of DC-DC converter and further critiques MICs based on pertinent characteristics with the objective of identifying the gap in research based on topology and control.

Chapter 3 contains the methodology of this research. It describes the design of the topology involving the configuration, operation modes, switching pattern, components determination, energy management algorithm, and control strategy.

Chapter 4 presents the results of simulations and hardware laboratory characterisation study of the BITIHGC proposed in this research. The simulation and experimental results are shown to indicate the converter response to different scenarios. These results are explained and discussed. Comparison with contemporary works was also done.

Chapter 5 presents the conclusions and recommendations for future work.

# CHAPTER 2

# LITERATURE REVIEW

## 2.1 Overview

This chapter provides information on the fundamentals of the DC-DC converter. It begins with a description of the basic single input converter after which the previous investigations on MICs are examined based on the level of isolation between the various input ports, and the output port(s). A review of the MICs and different control strategies leads to the establishment of the study gap as presented.

## 2.2 DC-DC Converter

The DC-DC converter as a power electronic converter takes in DC voltages at the input and delivers DC voltages at the output. The voltage and current levels at the respective input and output depend on the type of DC converter used. These voltage and current levels may be lower or higher at the input with respect to the output. The basic flow for a DC-DC converter is presented in Figure 2.1. The power source supplies to the converter which is regulated by the control unit and then to the load.

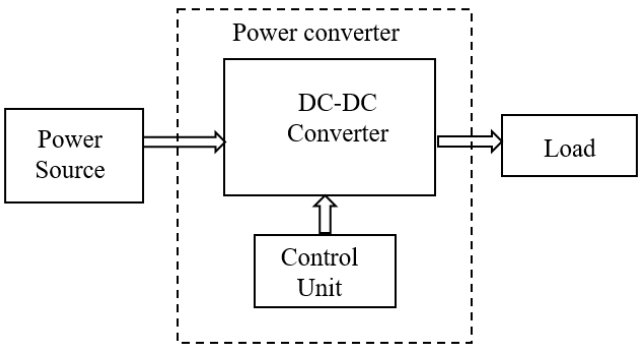


**Figure 2.1:** Block Diagram of a DC-DC Power Converter

### 2.2.1 Fundamentals of DC-DC Converter Circuit

Three basic topological structures of pulse width modulated (PWM) converters were initially identified (Mohan et al., 2003). They are the boost converter, buck converter and buck-boost converter. Additional basic topologies that were later developed are Cuk converter, single ended primary inductor (SEPIC) converter and the Zeta converter.

Inside the DC-DC converter, there can generally be three portions. The input portion, the output portion and the energy buffer portion. The input portion and the output portion take in voltage from the source and deliver voltage to the load respectively. The energy buffer portion utilises the capacitor and inductor to serve as energy buffers (Mohan et al., 2003). The buck converter, presented in Figure 2.2, delivers to the output portion, a voltage level that is less than the voltage fed to the input portion.

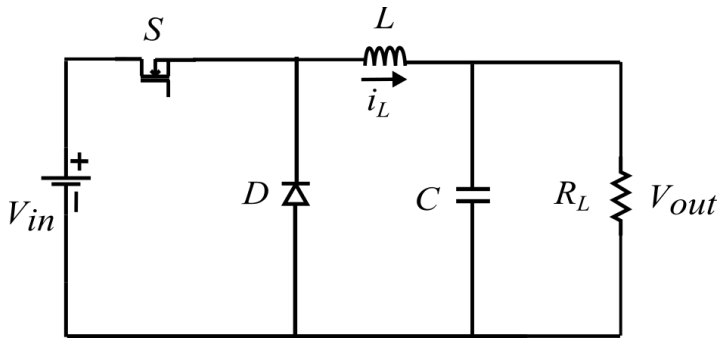


**Figure 2.2:** A Buck Converter (Mohan et al., 2003)

The boost converter negates the operation of the buck converter by delivering a higher voltage than the supply voltage. An alternate nomenclature of the boost converter is the step-up converter (Dileep & Singh, 2017). The buck-boost converter has the capabilities of the two previously mentioned converters and can deliver either lower or higher voltage to the load. It should be noted that the output voltage of this converter is negative in polarity.

The boost converter presented in Figure 2.3 show that the components are an active MOSFET power switch, *S*, a passive diode switch, *D*, an inductive element, *L*, a capacitive element, *C* and a load represented by the resistor, $R_L$. These components are basic to all types of DC-DC converters. The voltage conversion ratio of the basic converter is directly dependent on the 'turn-on' and 'turn-off' periods of the active power switch.

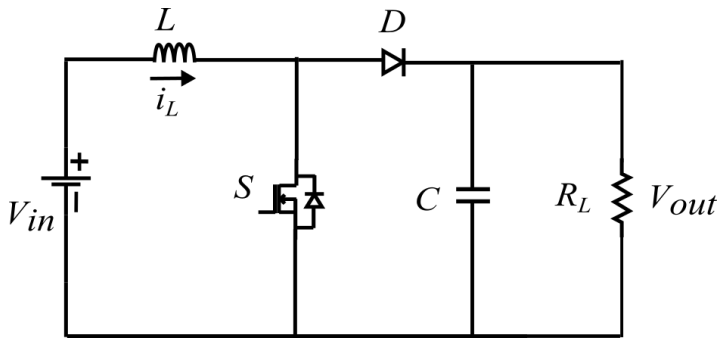


**Figure 2.3:** A Boost Converter (Mohan et al., 2003)

For the boost converter, when the switch closes, there is an increase in the inductor current due to charge from $V_{in}$ and this causes it to store energy (Mohan et al., 2003). The diode is reversed biased and the load is served by the capacitor during this period. When the switch opens, the conduction of energy stored in the inductor to the load is completed through the diode. The diode is the uncontrolled switch. This process is similar in the buck-boost converter except that the inductor is charged when the switch is open. The buck-boost converter is depicted in Figure 2.4.

In DC-DC converters, the mode of operation depends on the behaviour of the inductor current. There are two major modes. These are the continuous conduction mode (CCM), and the discontinuous conduction mode (DCM). The primary disparity between both modes is illustrated. During the CCM as shown in Figure 2.5, the value of the inductor current is sustained above the zero level all through the switching period. This is the opposite

during the DCM as shown in Figure 2.6. Here, the inductor current value plunges to zero value during the switching period.

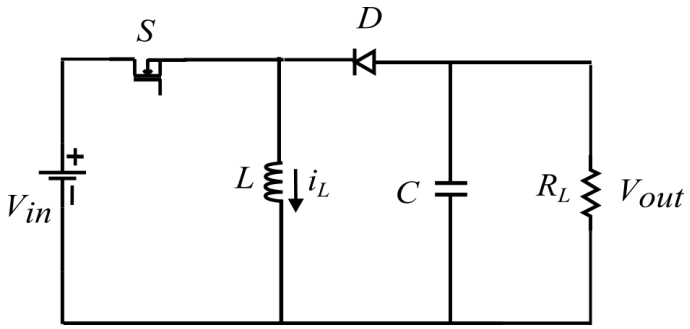


**Figure 2.4:** A Buck-Boost Converter (Mohan et al., 2003)

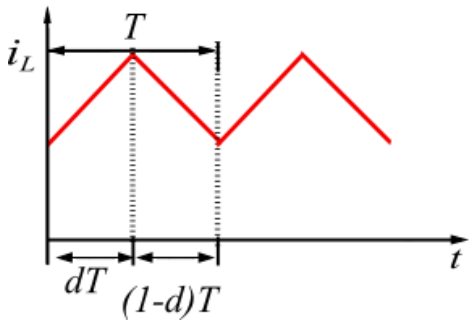


**Figure 2.5:** A CCM Inductor Current Waveform (Mohan et al., 2003)

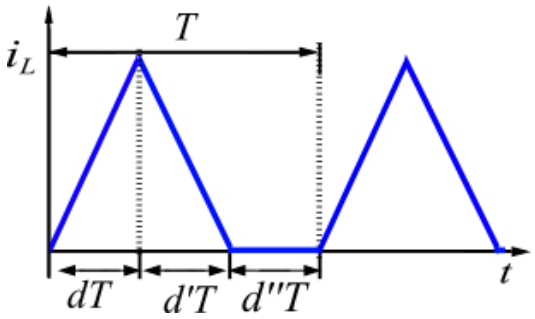


**Figure 2.6:** A DCM Inductor Current Waveform (Mohan et al., 2003)

The DC-DC converter is expected to deliver regulated voltage or current to the load. This implies that there must be a method of monitoring the output voltage or current delivered and subsequent adjustment of the variables and parameters. A closed loop feedback controller has been used for obtaining the desired voltage regulation. Mitchell (1988) identified the control gain and the controlled variable as two components of this control system.

### 2.2.2 Voltage Regulation of a DC-DC Converter

To attain the regulated output voltage, most DC-DC converters utilise a closed-loop feedback controller. In the feedback control scheme, the control gains and controlled variable are important elements. The inductor current and the output voltage are the controlled variables for a DC-DC converter. The controlled variable can be described as the variable that must be steadied relative to the set reference value (Rodriguez & Imes,1996).

The main aim of the controller, is to ensure that any errors that appear in the controlled variables, are corrected in a well-balanced manner in the quickest possible time. This is accomplished by manipulating the controlled variable. (Tse & Adams,1990). For control gains, they are used to boost the variables to desired levels.

The most common approach to control convenient for DC-DC converter voltage regulation is the fixed-frequency PWM control. This is mainly because there are a myriad of very cheap sophisticated fixed-frequency PWM controllers. Figure 2.7 displays the equivalent circuit for the DC converter's voltage mode control.

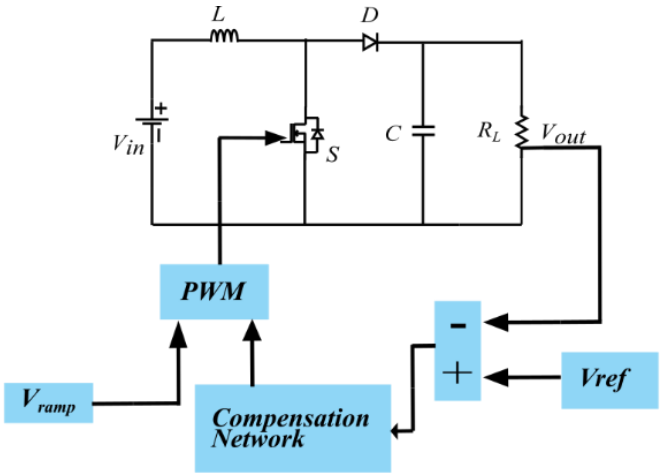


**Figure 2.7:** An Equivalent Circuit of Voltage Mode Control (Kapat & Krein, 2020)

The control displayed is a single-loop voltage mode control. The output voltage is regulated by a closed feedback loop that exists between the duty ratio signal and the output voltage. When the output voltage is compared to a continuous reference signal, *Vref*, voltage errors are produced. The compensation network then processes the voltage errors to provide a control signal (Mitchell, 1988). The required switching signal for driving the power switch, is generated by the PWM modulator based on the compensated control signal received.

## 2.3 Multiple Input DC-DC Converters

The need for the MIC increased mainly with the application of renewable energy sources. There is also the electric vehicle industry that is constantly seeking to optimise the utilisation of alternative sources and energy storage technology. The architecture of an MIC shown in Figure 2.8 has been proposed in diverse applications to tackle the previously highlighted drawbacks of series or parallel connected single-input single-output (SISO) converters. In the illustration, the power from the various input sources is routed to the common converter thereby diminishing cost via the achieved central control of variables.

This converter exhibits good source utilisation, compact size, and requires a smaller number of conversion stages and devices.

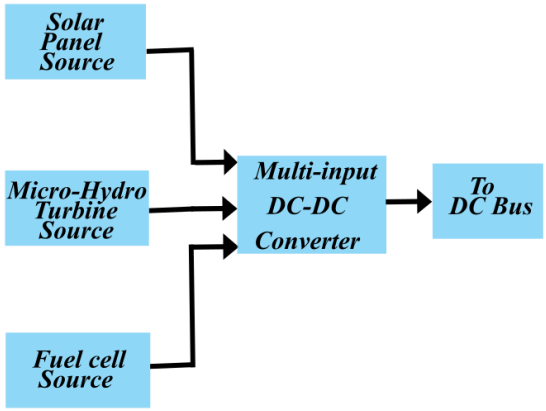


**Figure 2.8:** Outlay of a Multiple Input DC-DC Converter (Khosrogorji et al., 2016)

The early attempts to combine more than one input source in DC-DC converters resulted in connecting the sources serially or in parallel. An illustration of the series-connected MICs is presented in Figure 2.9. There are different voltage conversion levels for each converter, hence the respective voltage sources have a dedicated DC-DC converter that is controlled individually. These can be classified as an operation of different SISO converters to fill the gap. In similar pattern, the parallel connection of SISO converters is illustrated in Figure 2.10. The series connected converters may experience high power loss due to a potential circulating current. The respective outputs of the converters are terminated on a common DC bus (Kim et al., 2008). Historically, the complexity of having separate control for each converter may be further aggravated by the addition of communication drives to manage power in the parallel connected converter (Hui et al., 2010). Generally, the connection in whichever pattern, imply larger size, more losses and greater cost.

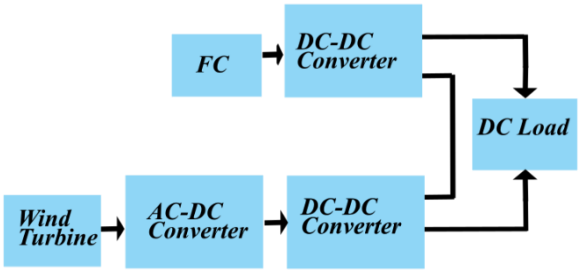


**Figure 2.9:** A Series Connected Multiple Input DC-DC Converter (Khosrogorji et al., 2016)

SISO converters can be classified based on their isolation status of the input and output. Thus, the two classes are the isolated and non-isolated DC-DC converters. Isolation in this regard, implies the existence of a transformer winding between the input and output. This winding facilitates the transfer of power from the input port to output port. The non-isolated converter does not have a transformer winding between the input and output ports. These ports share a common ground. The isolated converter has some advantages over the non-isolated converter. Isolated converters have higher voltage gain, good voltage matching and noise filtering. The disadvantages of isolated converters are large size and higher cost. Non-isolated converters have high power density, are cheaper and smaller in size. Classification of MICs can be based on the levels of isolation between the respective input ports and the output ports. These categories will be discussed and reviewed in the subsequent subsections.

### 2.3.1 Magnetically Connected Multiple Input Converter

Magnetically connected MICs are ‘fully’ isolated converters. In such a MIC, all the input ports and output ports are fitted with transformer windings which isolate them from one another. This is a fundamental advantage of this type of MIC. The voltage gain of these MICs are determined by the turns-ratio of the transformer winding. Another attractive feature of this type of MIC is the ability to load different values of voltage on the respective

input ports. The MIC is illustrated in Figure 2.11. It shows that input port one is not connected electrically to either input port two or the output port.

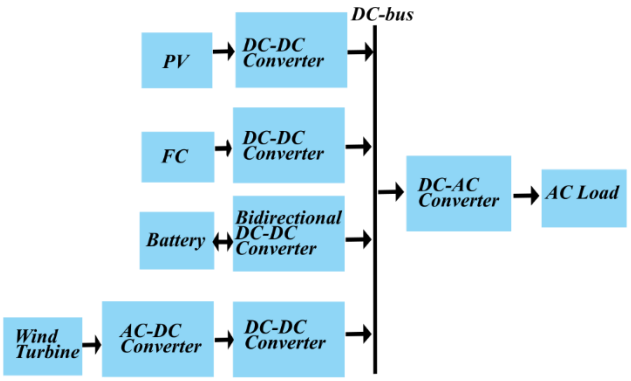


**Figure 2.10:** A Parallel Connected Multiple Input DC-DC Converter (Khosrogorji et al., 2016)

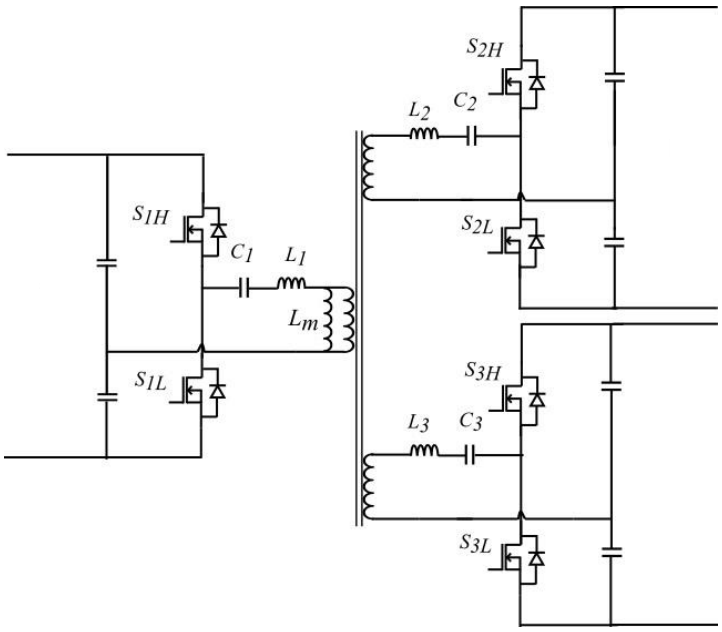


**Figure 2.11:** A Magnetically Connected Multiple Input DC-DC Converter (Tran et al., 2019)

### 2.3.2 Electromagnetically Connected Multiple Input Converter

In this category of MIC, the basic isolation exists only between the low voltage side and the high voltage side. The respective input ports have an electrical connection hence isolation between the input ports is non-existent. An illustration of such a MIC is presented

in Figure 2.12. The transformer turns ratio and the duty ratio of the power switches on the input side of the transformer determine the voltage gain of the MIC.

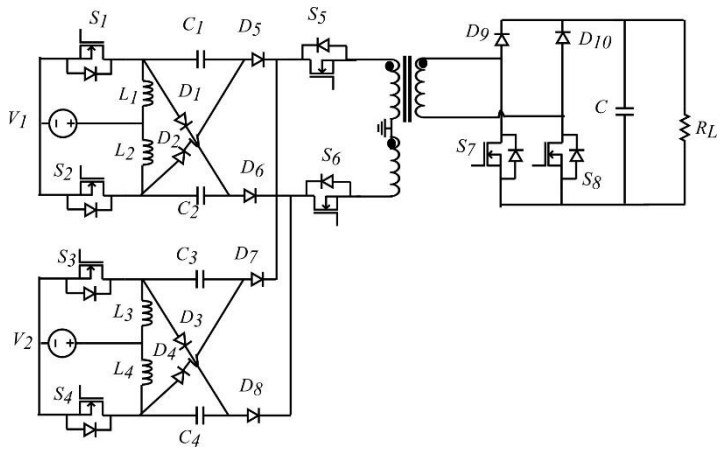


**Figure 2.12:** An Electromagnetically Connected Multiple Input DC-DC Converter (Raizada & Verma, 2018)

### 2.3.3 Electrically Connected Multiple Input Converter

In this class of MIC, there is no galvanic isolation between the various input ports in addition to the absence of isolation between the input ports side and the output port of the MIC. The voltage gain of such MICs rely on the duty ratio of the power switches. An example is depicted in Figure 2.13.

## 2.4 A Review of Multiple Input DC-DC Converters

Since RE sources are known to suffer from unavailability and low output voltage, the MIC emerges as the ideal contender for harnessing the merits of the RE sources optimally. A primary benefit of applying the multiple input topology is lower cost as compared to the series or parallel connected converters. Other benefits are simple management of RE resources and high power density. Over time, diverse research works

have been carried out on the MIC topologies. Some of these works will be critiqued hereafter.

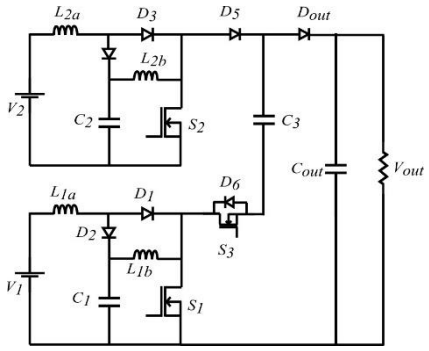


**Figure 2.13:** An Electrically Connected Multiple Input DC-DC Converter (Mohammadi et al., 2019)

### 2.4.1 Previous Research on Magnetically Connected Multiple Input Converters

The presence of the transformer winding in the magnetically connected MIC implies that leakage inductance is applied to transfer power between the primary part and the secondary part of the MIC. Many MICs can have some similarities in design. The magnetically connected MICs that have been investigated and proposed in the literature, can be grouped as discussed hereafter.

#### 2.4.1.1 Multiple Input Converter with Buck-boost Configuration

An early topology was a simple buck-boost configuration proposed as illustrated in Figure 2.14 (Matsuo et al., 1993). The input sources are two DC sources. With three operating states, the transformer functions as the inductor, thereby delivering aggregate fluxes for the input sources. The major demerits of this converter are unidirectional operation and its inability to deliver power to the load at the same time from the two sources. A battery

recharge capacity was included by Chen and Liu (2001). Further work on this buck-boost configuration used a PV panel and an AC line as input sources (Kobayashi et al., 2006).

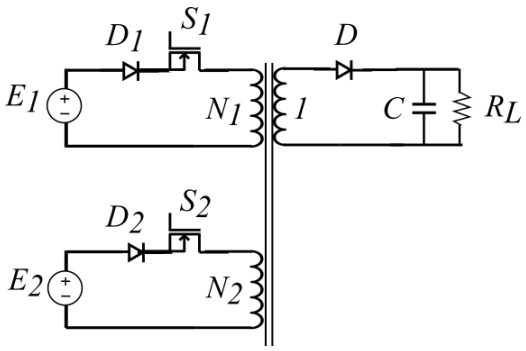


**Figure 2.14:** An early Buck-Boost Multiple Input Converter (Matsuo et al., 1993)

2.4.1.2 Multiple Input Converter with Full Bridge and Half Bridge Configuration

The application of full bridge and half bridge switch configurations has been investigated. The converter applied two current fed inputs with respective full bridge switch configuration (Chen et al., 2002). The output side employed a full bridge diode rectifier. The converter is shown in Figure 2.15. The operation of this converter is based on the principle of flux additivity. A phase shift of $180^{o}$ is applied to the complementary switches of the legs that form a half bridge. While the converter enjoys soft switching as a merit, it is cost prohibitive due to the high number of semiconductor devices required. Another demerit is the absence of bidirectional operation. This bidirectional operation was investigated by Krishnaswami and Mohan (2007). The insertion of an inductor linked full bridge switching configuration on the output helped achieve the bidirectional operation. The full bridge converter proposed in Zhang et al. (2012) incorporated four distributed transformers and secondary rectifiers in a manner that the input ports can easily be decoupled.

Increasing the number of inputs for the full bridge-based converter has been investigated. The four-input converter was achieved by adding windings and a full bridge rectifier (Falcones et al., 2013). Another method used four H-bridges with a high frequency transformer (Gao & Jiang, 2016). Other attempts to optimise this group of converters have been investigated. A resonance tank in series with the secondary winding part was added for soft switching (Suetomi et al., 2011). The optimisation of double input full bridge was investigated (Li et al., 2011). Another author focused on the control strategy for the full bridge converter (Yang et al., 2009). The half bridge topology was discovered to have less complexity of control unlike the full-bridge topology that is associated with a high number of devices. Depending on the design of the switching signals, the half bridge topology can be described as asymmetric or symmetric (Mao et al., 2004).

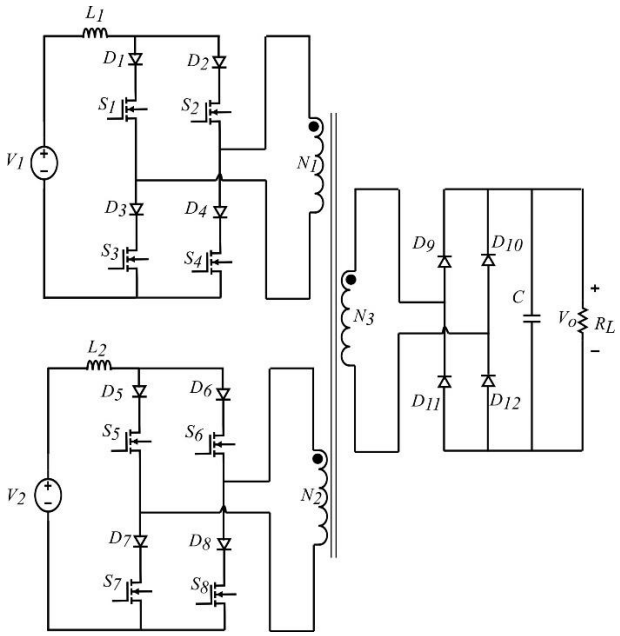


**Figure 2.15:** A Flux Additivity Based Full Bridge MIC (Chen et al., 2001)

#### 2.4.1.3 Bidirectional Multiport Converters

The bidirectional multiport converters in this category can adopt any of the inputs as the load. The triple half bridge configuration has been proposed (Tao et al., 2008). The half bridge inputs are tied to a fuel cell and a supercapacitor respectively. The supercapacitor serves as the storage. The supercapacitor port is current-fed. This results in low current ripple. External capacitors are placed after the half bridges. An advantage of this converter is the presence of soft switching without the need for additional circuitry at high frequency.

The development of an asymmetrical triple active bridge from the dual-active bridge was investigated by Jakka et al. (2017). On the primary side, full bridges were attached to separate transformer windings while the secondary side gained a three-leg converter. Although this reduced the leakage power, the drawbacks are the number of switches and convoluted control. Other bidirectional multiport configurations have been proposed. The soft switching at low frequency was implemented by snubber capacitors and the transformer leakage inductance (Liu & Li, 2006). A similar half bridge configuration was proposed for lamp ballasts (Liu et al., 2010). The full bridge configuration was adopted for FC and two storage devices (Phattanasak et al., 2015). Resonant tanks have been included in some configurations to achieve zero current switching (ZCS) and zero voltage switching (ZVS) conditions (Liu & Li, 2019; Tomas-Manez et al., 2017; Tran et al., 2019; Wang et al., 2018).

#### 2.4.1.4 Double input full-bridge boost converter with multi-winding transformer

Zhang et al. (2011) proposed the double input full bridge converter structure. For a particular input port, the associated boost inductor forms a current source. A full bridge inverter is placed next to the input stage. On the primary part, the four transformer windings possess equal turns ratio. On the secondary part, two full-bridge rectifiers sandwich another four transformer windings. During two of the three operating modes, concurrent delivery of

power to the load is not attainable. Zhang et al. (2012) focused on investigating the mechanism to increment the input ports to the converter as well as noise attenuation, and reduction of magnetic parts. A lower efficiency is evident due to the high parts count.

### 2.4.2 Previous Research on Electromagnetically Connected MICs

As stated earlier, the electromagnetically connected MIC does not have isolation between input ports. The isolation exists only between the low voltage side and the high voltage side. The connection between the input ports can be described as a DC link.

#### 2.4.2.1 Double Input Converter

A direct charge converter has been proposed (Wu et al. 2011a). The converter contains a battery port on the DC link. It makes use of half bridges on either side of the transformer. It is able to operate in double output mode during which the battery can be charged. The converter's merit is the low switch count. The authors further developed a family of DC-linked converters. This group of converters have individual synchronous and post regulation capability (Wu et al. 2011b).

The converter proposed in Tao et al. (2005) is ideal for FC and supercapacitor inputs by making use of current fed half bridges. One half bridge on the primary side combines with another half bridge on the secondary side to fashion a dual boost half bridge. The half bridge tied to the supercapacitor is bidirectional. Wu et al. (2016) introduced a mid-tapped transformer and removed the capacitors saddled between the half bridges and the primary winding. The ZVS properties in the boost and phase shift controlled full bridge converter were investigated (Al-Atrash et al. 2006). The relocation of the secondary side half-bridge to the primary, was proposed to obtain a boost-integrated full bridge converter (Al-Atrash & Batarseh, 2007). The switches can only turn-on in an alternate sequence and at the same duty

ratio in order to avoid a short circuit. This result in limited output voltage by the MIC. Raizada and Verma, (2018) merged the interleaved inductor technique and voltage multiplier (VM) cells on the primary side ports to achieve a high voltage gain. However, the high switch count is the demerit of the MIC. The converter proposed by Gunawardena et al. (2023) used full bridges on the secondary side. The converter has two current fed input ports. The application of the DCM operation for the main inductors along with secondary side modulation helped to achieve soft switching for the converter.

#### 2.4.2.2 Tri-modal Half Bridge Converter

The converter proposed by Al-Atrash et al. (2007) can identify as a tri-modal half bridge converter. The half bridge source in addition to the active-clamp forward source are the suitable input ports. A distinct feature of this converter is that the transformer has the free-wheeling diode as well as the switch branch astride it. This converter can charge the battery, employ soft-switching and marginally reduce the stress on the switches. The battery charge and discharge cannot be controlled. Further work on the converter achieved battery charging control by infusing a capacitor, between the battery terminal and ground (Qian et al., 2010a). This capacitor infusion, permits a higher degree of control for battery operation. The number of inputs for the converter was extended to four input ports to accommodate RE sources and battery storage (Qian et al., 2010b).

#### 2.4.2.3 Multiple Input Converter with Simultaneous Power Management

The converter proposed by Zeng et al. (2014), incorporated maximum power point tracking converter capabilities to elevate the input voltage. A schematic of the MIC is presented in Figure 2.16. The MIC is suitable for various RE sources. Some examples are wind turbines, PV, and FC. The MIC possesses boost function in three operating modes. Single source power transfer is possible by allowing only a single switch to conduct while

every other switch does not conduct. Simultaneous power delivery from all the RE sources occurs when every switch does not conduct. Jiya et al. (2021) proposed an MIC based on the flyback converter. Each input module consists of a voltage source connected in series with a switch. The input modules are connected in parallel. A clamping circuit follows the input module. The converter can deliver a high voltage gain in buck or boost mode. The output voltage is non-inverted.

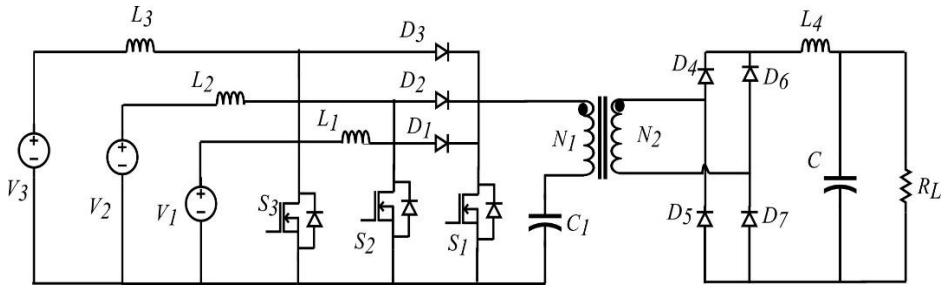


**Figure 2.16:** A Multiple Input Converter for Simultaneous Power management (Zeng et al., 2014)

2.4.2.4 Three Level Multiple Input Converter

The MIC proposed by Dusmez et al. (2016), inserted pulsating current-source cells (PCSC) at the input ports. On the primary part of the winding, a three-stage structure subsists. The full bridge converter serves on the secondary part of the winding. Although the MIC can control the output from the input sources, it cannot control the battery charge or discharge process.

2.4.2.5 Multiport Boost Converter with Isolated and Non-Isolated Ports

A converter that contains the isolated port and the non-isolated port was advanced by Zhu et al. (2015). The authors combined a modified half bridge proposed by Al-Atrash et al. (2007b) with a boost topology. The body diodes of selected switches enable freewheeling of primary current. The advantages are continuous input current as well as ZCS

operation. Kishore and Bhimasingu (2018) added the AC output port to the ports by infusing three parallel legs. The three-port converter proposed by Zolfi et al. (2021) used a SEPIC configuration on the secondary side. The battery and bidirectional load port are placed on the secondary side of the transformer.

#### 2.4.2.6 Zero Current Switching Based Multiport Converter

Nareshkumar et al. (2016) proposed a ZCS converter. This converter uses a resonant tank based on a parallel resonant capacitor and transformer leakage inductance. The current fed input implies that the converter can serve some types of RE sources. Later improvements by Reddi et al. (2018), comprised the 5-level inverter and resonant capacitor. The low number of switches is the merit. The drawback is the complex control requirement. Lin et al. (2018) proposed the removal of the resonant tanks. Dual PCSC input ports make up the primary part while the full bridge completed the secondary side of the transformer. By this method, the converter can become a four-port converter. Soft switching and the high VTR are evident in the MIC. The high number of semiconductor devices is a demerit for this converter. The full bridge three port converter was advanced by Wu et al. (2012). It has a wide range of input voltage. The major drawback of this converter is high losses.

#### 2.4.2.7 Connective Storage Based Bidirectional MIC

The propounded MIC combined connected battery banks at multiple input ports (Karthikeyan & Gupta, 2018). The MIC is bidirectional and the battery banks are connected in series. A bridge stage follows the series battery bank on both the primary part and the secondary part of the transformer. This is a modified dual active bridge configuration that improved efficiency by reducing circulation power and peak stress. Bidirectional operation is a feature of the MIC. The converter can function as a single input or combined input depending on the switches and anti-parallel diodes. The semiconductors' count increments

as that of the number of input ports. In addition, a complex control strategy is required for the battery bank.

### 2.4.3 Previous Research on Electrically Connected Multiple Input Converters

#### 2.4.3.1 Synthesis of Electrically Connected MICs

It is essential to highlight several authors who have proposed various methods for developing electrically connected MICs. Kwansinski (2009) investigated the feasibility of mutating several conventional converters with one input port to MICs. The author propounded four rules for developing an MIC. However, these rules can only adapt buck and buck-boost converters to MICs. Liu and Chen (2009) proposed a model for a pulsating source cell (PSC). A PSC could be either a pulsating voltage-source cell (PVSC) or a PCSC. Adding PSCs to the basic PWM converters contrived multiport converters that can accept different sources.

Li et al. (2010) determined that the output filter cell (OFC) and the PSC are the primary parts of MICs. The authors went further to identify classes of PCSC, PVSC and OFC. Two variants of MICs were developed using several PSC and OFC combinations. Such concept can suffice in magnetically connected and electromagnetically connected MICs. The work done by Chen et al. (2018) was limited to fusing ‘single-input double-output’ and ‘double-input single-output’ models for traditional converters. Kumar and Jain (2013) provided more insight on the application of PSCs in developing MICs. Shan et al. (2021) proposed a set of rules for developing multiple inputs and multiple outputs (MIMO) converters that do not require energy buffer stages. It involved fusing the PSCs into a module that is connected to an OFC module. The authors investigated the suitability of three OFC configurations.

2.4.3.2 Parallel and Series Connected DC-DC Converters

The foremost attempt at developing non-isolated MICs proposed the parallel and series connection of converters. Solero et al. (1996) suggested the electrical linkage of boost converters in a series topology. The converter is shown in Figure 2.17. The applicable RE sources are PV and the wind generator. The parallel coupling of buck converters was proposed by Imes and Rodriguez (1994). The authors investigated the dynamic behaviour as well as the stability of the converter (Rodriguez & Imes, 1996). Parallel coupling was investigated (Di Napoli et al. 2002). The converter can deliver boost and buck functions. Hence, it has an edge over Imes and Rodriguez (1994), and Rodriguez and Imes (1996). The demerit is the absence of soft switching.

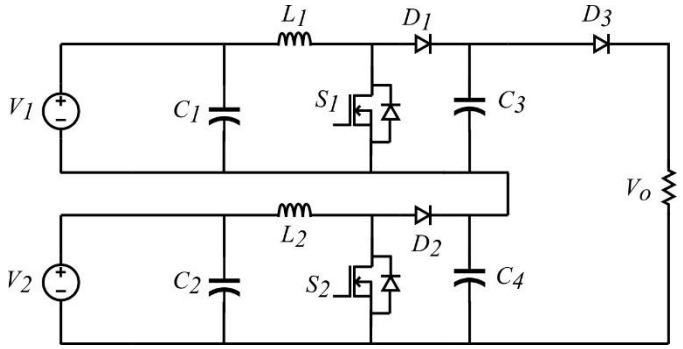


**Figure 2.17:** Series Connected DC-DC converters (Solero et al., 1996)

Solero et al. (2005) modified the converter and devised distinct buck or boost operation for the respective input units. The converter is shown in Figure 2.18. The capacitor count is lower because a common output filter was used. Zhang et al. (2014) enhanced the converter efficiency by removing the DC-link capacitor in a parallel connection of buck/boost cells. This converter is bidirectional. Majumder and Bag (2014) investigated the control of the converter with focus on integrating several microgrids.

A family of converters using series or parallel connections of different configurations has been proposed (Wu et al., 2015). The double input converter (DIC) is dedicated to battery charging by Chen et al. (2015), used a parallel connection between the comprising forward converter and buck/boost converter. The voltage summation approach was proposed in a switched diode-capacitor converter (Hou et al., 2016). Addition of the input voltages resulted in higher output voltage. Jananie and Rajambal (2017) investigated the performance of the converter.

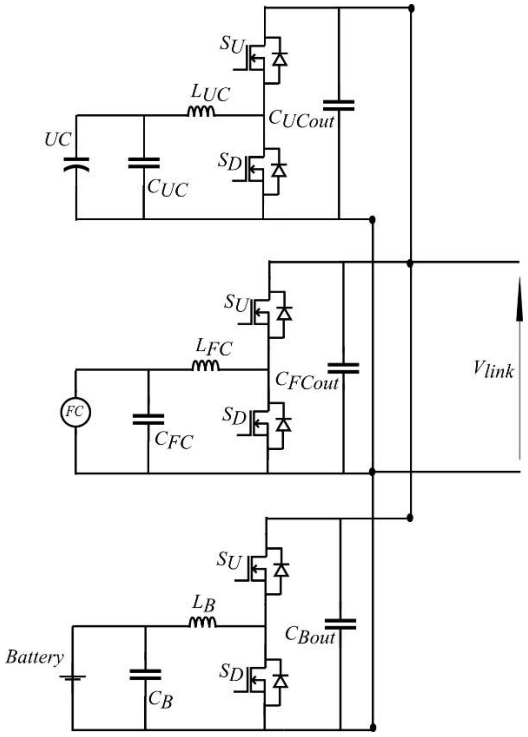


**Figure 2.18:** Parallel Connected Converters (Solero et al., 1995)

2.4.3.3 Double Input DC-DC Converter

The DIC is quite ubiquitous among non-singular input DC-DC converters. Chen et al. (2006) modified the conventional buck-boost and buck converters to accept binary voltage sources. A schematic of the DIC is depicted in Figure 2.19. The input sources are one low voltage source and another high voltage source. The output voltage cannot be more

than the high input voltage or less than the low input voltage. This DIC is equipped with soft switching, and can produce voltage levels without transformers. The limitation of the maximum output voltage limited to the highest input voltage is a demerit. A solution was proposed in Kanhav and Chaudhari (2017) by insertion of a magnetic element in the PVSC arrangement. When either or both switches conduct, power is transferred from either or both sources to the output. Another investigation added the bidirectional feature to the DIC. A third switch replace the upper diode to attain this functionality (Kanhav & Chaudhari, 2018).

The DIC proposed by Yalamanchili et al. (2006) applied two PVSC cells to the two inputs of an integrated buck-buck converter. A buck-buckboost DIC was devised by creating a ground loop to the inductor output. Gummi and Ferdowsi (2008a) proposed DICs formed from the single-pole-triple-throw switch. A similar work used H-bridges to build the DIC (Gummi & Ferdowsi, 2008b). The DIC in Prabhala et al. (2009) uses the buck-boost/buck-boost configuration. The charging time of the inductor determined the output voltage. The DIC is suitable for battery charging.

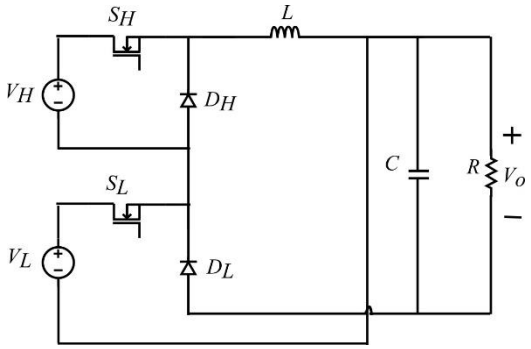


**Figure 2.19:** A Double Input DC-DC Converter (Chen & Liu, 2002)

The DIC proposed by Akar et al. (2016) merged the buck-boost/buck configuration. It is suitable for the battery system of electric vehicles. A bidirectional DIC by Vural (2013)

used the coupled inductor topology. This design improved dynamic response of the FC and ultracapacitor. In Akar et al. (2018), the conditions are such that the input sources of the DIC can either deliver to the output, or charge one of the input ports at a time. A PV-battery system is a good application for this converter. The input port count increased by fixing the switch-diode branch to the inductor.

The buck/buck DIC proposed by Sun et al. (2015) can be termed as a bootstrap circuit. The buffer portion of the converter is connected in series with a charging switch. The converter has a high fault tolerance in the event of a short-circuit of any input port. Two switches in a special combination achieved simultaneous power transfer (Park & Kim, 2017). The wide input voltage range of the converter is notable even though power delivery by a single input source required an auxiliary diode. A weakness of the converter is that a threshold voltage is required for the secondary input to power the load.

The buck/buck DIC introduced by Muntean et al. (2011) achieved soft switching by interfacing the input ports with inductor-capacitor (LC) circuits. Gavris et al. (2011) interchanged the inductor and capacitor branch positions. Further investigation was conducted on the DIC performance in boundary conduction mode (Gavris et al., 2014). The dual LC converter was developed by merging the capacitor buck cells with the hybrid inductor (Gavris et al. 2012). Cornea et al. (2012) investigated the LC buck DIC in standalone mode. The PV and wind turbine are the applicable RE sources. Muntean et al. (2012) integrated the LC converter with a grid system.

Veerachary (2009) investigated the integration of parallel connected SEPIC-buck DIC. The DIC has lower number of components. A steady-state analyses of the DIC was done by Kumar and Veerachary (2013). The DIC by Veerachary and Trivedi (2022) applied

the boost cascaded charge pump method. The input ports provide continuous current as they are in series with the inductors. The converter is a less complex structure.

Harini et al. (2022) used a Z-Quasi Resonant network to reduce the voltage stress of the dual input converter. The converter is suitable for electric vehicles and microgrids. Ali Khan et al. (2019) connected the secondary battery storage in parallel to the input ports. Battery charging from the input ports is feasible. Voltage boosting is via the regular boost method. There is a low number of components.

Several DICs that use a blend of the regular converters have been proposed. Moury et al. (2016) introduced the soft-switching feature in a buck/buck DIC just as Zhao and Kwasinsky (2009) proposed a SEPIC/ SEPIC structure thus forming a double input SEPIC converter. Haghigian et al. (2017) added the battery function to the dual input ports of the SEPIC converter. Sun and Bae (2017) equipped the Cuk DIC with edge-resonant soft switching thus, improving the efficiency. The multiple input Cuk converter proposed by Moury and Lam (2017) used resonant switches to control each input port. The converter proposed by Wai and Hong (2014) used a boost structure to attain a high step-up function. The double input and double output converter benefited electric vehicles (Suresh et al., 2021). The current fed port is in parallel with the battery port. A unidirectional output port is tied to the battery port while the bidirectional output port is connected in parallel to the battery and primary input port. The converter uses boost and buck-boost configurations.

#### 2.4.3.4 Multiple Input Buck-Boost Converter

A parallel connection of the input sources was proposed by Dobbs and Chapman (2003). The buck-boost configuration is placed after the power control switches. The converter has uncomplicated control and low number of components. Some demerits are the

negative output voltage, lack of concurrent supply by the input sources, negative reference output voltage and no bidirectional capability. A solution to the negative output voltage and bidirectional operation was proposed by Khaligh et al. (2009). The authors added two extra switches to the MIC. The circuit is presented in Figure 2.20. It can work in the boost, buck and buck-boost modes. Simultaneous power deliver is possible during the buck mode only.

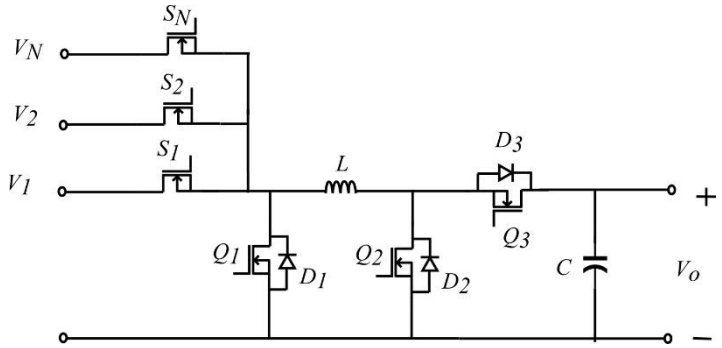


**Figure 2.20:** A Multiple Input Bidirectional Buck-Boost Converter (Khaligh et al. 2009)

2.4.3.5 Diode-capacitor/Switched-capacitor/ Switched-inductor Based MIC

Ye and Cheng (2012) investigated the feasibility of zero use of magnetic elements based on switched capacitors (SC). The DIC contains three switches which operate at fifty percent duty ratio. Subtracting the input voltages will give the output voltage of the DIC. The converter experienced high output ripple in addition to an equally high output leakage voltage. The converter is a multi-input voltage subtraction converter. A similar converter is the multi-input voltage summation converter (Ye & Cheng, 2013). The elements have been rearranged such that the output voltage is the sum of the input voltages.

The converter proposed by Hou et al. (2016) fits the series connected DIC description. However, the technique of aggregating voltage by switched-diode capacitors was investigated. The characteristics are similar compared to Ye and Cheng (2012). The

switch voltage stress and current stress values are low. Jananie and Rajambal (2017) investigated the series-parallel variations. Shoaei et al. (2022) used a single inductor in the energy buffer. The PVSC inputs are series connected. The total output voltage is the sum of the output of each capacitor diode circuit.

Shekin and Biju (2021) proposed the bidirectional MIC based on switched capacitors. Each input port is connected in series with two switches. The positioning of the switches is such that the body diodes are in opposite direction. Thereafter, a single inductor stage is followed by the cascaded switched capacitor configuration. The input ports are joined via a parallel connection. The converter has reduced number of inductors, low switch stress, and high voltage gain. A weakness is the losses due to passive components.

Akar and Kale (2018) proposed the arrangement of the SC cells in a multilevel structure. The input ports are current fed input, thereby keeping input ripple low. The MIC delivered a high voltage gain due to the SC cells. A demerit is that the number of passive elements is high. The similar MIC investigated in Khosravi et al. (2017) produced a lower voltage gain. This is because only one SC stage was implemented. In a four-port converter, Aravind et al. (2023) implemented an actively switched inductor capacitor network in order to increase the high voltage gain. The component count of this converter is low.

The voltage boosting method provided by switched inductors in MICs was investigated (Mahmoodieh & Deihimi, 2019). One notable property of the MIC is that battery charging from different input ports is possible. The duty ratios of the switches that control the input port do not affect the rate of battery charging and discharging. The efficiency of the MIC is high despite the high number of inductors.

#### 2.4.3.6 Buck/Boost-Boost Based MIC

The buck/boost as well as the boost converter have been combined by Banaei et al. (2014). The converter is robust due to its modularity. It also achieves independent control of the input sources. The MIC has low current stress and the control is uncomplicated. The drawback is that an increase in the number of input sources implies an increase in the number of semiconductors and magnetic elements. This also applies to the switches' voltage stress and current stress. The converter introduced by Chandrasekar et al. (2020) is suitable for PV storage. Two unidirectional ports suffice. The battery is connected to the bidirectional port. Buck and buck-boost techniques are used at the energy buffer stage.

#### 2.4.3.7 Bridge Type Dual Input Converter

Athikkal et al. (2019) investigated the bridge structure in dual input converter. This structure permits the singular and simultaneous delivery of power from the input sources to the load. Bidirectional operation is a property of this converter. A combination of switches and diodes can determine step-up, step-down, or both working modes. A performance analyses on an earlier unidirectional topology reveal efficient energy utilisation (Athikkal et al., 2017). The bidirectional operation can be realised by using the bidirectional switch in the position of the output diode. Kumaravel et al. (2018) used three relay switches to achieve bidirectional operation. This family of DICs are basic in structure, easy to control, have low number of components, and work in both directions. The converter faces some problems that are common with the traditional converters. Examples of these are high input current, output voltage ripple and switch voltage stress

#### 2.4.3.8 MIC Family with Three Switches Leg

Azizi et al. (2016) proposed a family of three-switch inverter structure having a current fed input. The number of inputs can be increased by adding legs and the

accompanying elements. An inverter is formed by the four uppermost switches. The converter outputs are AC and DC outputs with boost and buck functions. The converter can function in the step-up mode and step-down mode. The number of passive elements is low but there is no soft-switching.

#### 2.4.3.9 Three Port DC-DC Converter with Soft Switching

The converter proposed by Faraji et al. (2021a) used a single inductor for the energy buffer stage. Multiple ports can be added by connecting extra non-battery input ports in parallel. An included snubber circuit helped to achieve soft switching function. A different configuration of the auxiliary circuit is proposed in Faraji et al. (2021b). The converter was further modified to include the bidirectional function for all ports (Faraji et al., 2021c). However, coupled inductors were used to design the soft switching cell. Four different soft switching techniques were proposed for the highly integrated three port converter (Faraji et al., 2021d). While the presence of soft switching is good, implementation increased the converter size and cost. The three-port converter proposed by Dezhbord et al. (2022) also used the coupled inductor technique to facilitate ZCS. In addition, VMs based on coupled inductors have been used to increase the voltage gain of the converter.

#### 2.4.3.10 High VTR Multiple Input Converter

The high VTR MIC proposed by Amiri et al. (2021) used coupled inductors and a clamping circuit. The current fed input sources are connected in series. Saadatizadeh et al. (2021) proposed a high VTR MIC that can eliminate input current ripples. An input module containing coupled inductors are modelled like transformers to remove current ripples and increment the voltage gain. A merit of the converter is the low voltage stress on switches.

Another high VTR DIC based on the use of VMs was proposed (Prabhala et al., 2016). The VTR of the converter is 20. Diode-capacitor VM cells follow the two current fed input ports. The VM cells support the continuous input current thereby leading to a high voltage gain. The converter has simple control but lacks bidirectional capability. The number of passive elements is high and increases the dissipation losses. Hosseini et al. (2017) increased the number of VM cells and input ports. The converter has been extended to the MIMO setup in Mohseni et al. (2019). The auxiliary zero voltage transition circuit in Zhu et al. (2019) reduced the switching losses. The diode stress of the converter is lower despite the high number of diodes.

#### 2.4.3.11 MIC with ZVS

The MIC in Wai et al. (2011) made use of an auxiliary circuit to achieve ZVS for the switches. The inputs are current source type and can function as single input or dual input. The conduction losses are lower in the dual input state thereby resulting in high efficiency. However, in single input state, there is high voltage stress on the semiconductors. The auxiliary circuit in Wai et al. (2012) contains an auxiliary switch, inductor, capacitor, and parallel diodes. The efficiency of the MIC is high due to the ZVS operation. The design by Mohammadi and Moghani (2018) added an active clamp with the quasi-resonant buck-boost technique. In addition to ZVS, a high voltage gain was attained. The auxiliary circuits increase the number of parts.

#### 2.4.3.12 Modular High VTR MIC

The technique of stacking supplementary input ports on the main input port was proposed (Varesi et al., 2017). Each supplementary input port is accompanied by its own energy buffer elements. Hence, independent operation is possible for the respective input sources. The high VTR, low voltage stress on switches, and independent control of input

sources are the merits of this converter. A demerit is the increased parts count as the input sources increment.

Non-coupled inductors have been utilised in voltage boosting for the modular MIC with high VTR (Varesi et al., 2018a). The non-coupled inductors are assembled for the various input ports. The schematic is presented in Figure 2.21. The respective input and energy buffer portions share a common filter and bidirectional switch. Some merits of the MIC are ultra-high gain, bidirectional function and low normalised voltage stress on the semiconductors. Since there are fewer shared components, controlling the SISO converters is complex. The current stress on the bidirectional for battery charging switch is quite high (Varesi et al., 2018b). In the modular converter proposed in Gaurav et al. (2022), each additional input port is connected to an interleaved inductor branch in a cascaded structure. The primary input port is a boost converter lifted by a capacitor. It has a low voltage stress.

In Mohammadi et al. (2019) a voltage transfer ratio of 27.43 was achieved in a modular structure. The voltage stresses are less due to low duty ratio. In addition to the modular form, high voltage gain, the converter has a low average normalised peak inverse voltage (PIV). The disadvantage is the high number of components. In the grid-level MIC that was proposed by Moury and Lam (2020), each module has a Cuk and flyback-based circuitry. A battery storage system is also attached to each module. The quasi-resonant Cuk configuration facilitates soft switching. Saadatizadeh et al. (2022) extended the modular multiple inputs to the multiple output. An extra input can be added by stacking on a current fed input branch. For the extra output port, an additional diode is connected in series with the outermost inductor.

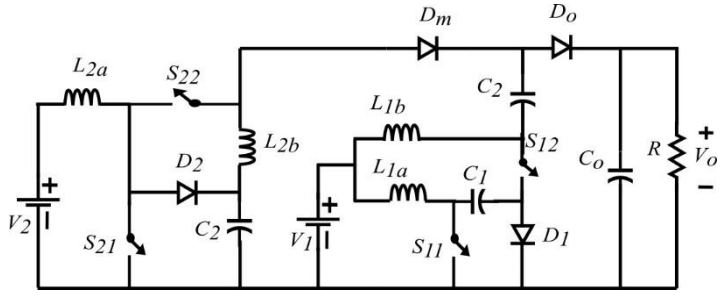


**Figure 2.21:** A Modular Bidirectional High VTR Multiple Input Converter (Varesi et al. 2018a)

2.4.3.13 MIC with Multiple Output

Some MICs with multiple output ports have been proposed in the literature. Such multiple output MICs are useful in electric vehicles and communication equipment. A single inductor was used in the energy buffer stage as proposed by Li et al. (2020). The input is a series connection of PVSCs leading to the energy buffer stage. Each output module is made up of a switch in parallel with an OFC. The respective output modules are connected in series. The switch in the output module makes independent control of the output possible. While this converter has an advantage of simple structure and easy loading of additional ports, it may not be suitable for applications that require a common ground.

Athikkal and Eswar (2021) proposed a three-input and double output converter. The respective input and output ports are connected in parallel. Hence, there is limited control of the output. The converter has a low parts count as only one inductor is used in the boost stage. In Nnachi et al. (2023), the single switch-connected input ports are connected in parallel. The design is a buck-buck converter. There is a single-inductor energy buffer stage. Each output port has a switch, diode and inductor connected in parallel. The converter has high power density and is reliable. It is expensive to use and suffers from high noise.

A switched-resonator MIMO architecture is proposed (Jabbari & Dorcheh, 2018). A regular resonant converter was modified to MIMO ports. This was done by linking a forward-conducting bidirectional-blocking (FCBB) switch to the resonator. The converter is shown in Figure 2.22. The FCBB switch also protect the ports from short-circuits. This architecture makes it easy to add bidirectional ports. The advantages of this converter are ZCS operation and easy power routing. There is increased number of switches and inductors as the number of ports increments.

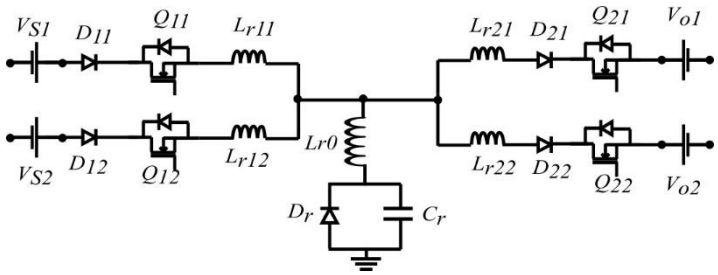


**Figure 2.22:** A resonant MIMO ZCS Converter (Jabbari & Dorcheh, 2018)

The MIMO converter proposed by Nahavandi et al. (2015) was optimised for electric vehicles with different load voltage requirements. A series-parallel connection of switches and diodes is applied to split the outputs. An FC is the primary input while a battery is the secondary input. For the converter to deliver to the output, the voltage level of the FC input must be higher than that of the battery input. Babaei and Abbasi (2016) proposed a boost converter and SC for multiple outputs. The multiple outputs are connected in parallel. In a scenario, the MIMO converter used a combo of the matrix outlay and the buck-boost structure (Jafari et al., 2012). For each output port, a regular buck-boost converter is fixed to the output capacitor. The output ports are not simultaneously powered by the input ports. The number of semiconductor devices is high.

The converter proposed by Gorji et al. (2019) utilised a parallel connection of the input sources. The interleaved technique was applied at the buffer stage and the multiple outputs were derived by simple voltage dividers. The parts count of this MIC is high. Saeed et al. (2018) proposed cascaded multiple outputs combined with separate switching units. The use of individual buffering elements attached to the respective units resulted in independent voltage for the output ports.

A SISO buck-boost converter can be fitted for MIMO operation (Khan et al., 2014). To include an additional input port, the authors proposed placing a module on the step-up side of the DC link capacitor. The module contains a half bridge paralleled with an inductor. Placing the module on the buck side of the DC-link capacitor facilitates additional output ports. The bidirectional feature makes it suitable for the vehicle-to-grid interface. The DIC proposed by Khan et al. (2018) had a PV input and a battery bank. The voltage gain is achieved by a conventional boost converter. Two output ports and bidirectional feature exist in the converter.

#### 2.4.3.14 Three-input battery-integrated boost converter for RE Sources

Feyzi et al. (2011) proposed a three-input converter for RE applications. Each of two primary input ports independently connected to a boost converter. The converter is shown in Figure 2.23. The input sources are PV cell and FC and battery. This battery storage is connected to a full bridge configuration. There is uncontrolled battery charge and discharge. This impacts negatively on the battery life. Ahrabi et al. (2012) removed the full-bridge converter while connecting the battery input in series with the PV input port. Two boost converters form the buffer stage of the converter.

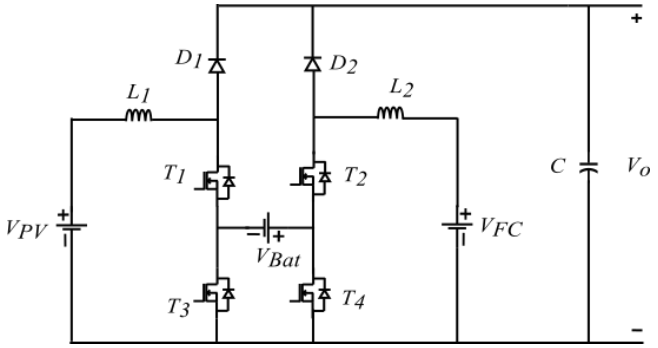


**Figure 2.23:** A Three Input Converter for PV/FC/Battery (Feyzi et al., 2011)

The converter proposed by Nejabatkhah et al. (2012) operates in three modes. The conditions for the first mode require a full battery state of charge (SOC), along with sufficient PV and FC power to satisfy the load requirement. For the second mode, the full battery SOC complements the PV and FC in serving the load. For the third mode, both the depleted battery and the load are serviced by the PV and FC ports concurrently. A converter that serves a bidirectional load was proposed (Ghavidel et al., 2019). A low frequency switch is used to achieve the bidirectional load function. This converter gain is low. Balaji et al. (2017) added three input ports to the converter.

Improvements to the three-input converter, dedicated the step-up configuration to the FC port, and the buck-boost configuration to the PV port (Kardan et al., 2017). The independent switches curtailed the arbitrary battery charging characteristic. The boost capacity is higher than that of conventional converters. There is increased dissipation loss due to the number of passive elements. Alizadeh Asl et al. (2022a) used two buck-boost converters to achieve continuous current for both the FC and PV input ports. Further work done by Alizadeh Asl et al. (2022b) improved the voltage gain, while maintaining the low component count. A mix of buck and boost converters was proposed by Aboreada et al.

(2019). The converter has few components and a simple switching pattern, but only one input source can charge the battery at a time.

## 2.5 Review of RE Applications using MICs

Some RE applications as used by MICs are presented in Table 2.1. It can be seen that MICs have transited from series/parallel connection of several converters to improved MICs that can deliver different types of output voltage. An example is the MIC that can simultaneously deliver DC and AC voltage output (Kishore and Basimangu, 2018). Such MIC is useful in battery electric vehicles, plug-in hybrid electric vehicles and high-power fast charging stations.

The most sought after RE sources for application in industry are solar energy, wind turbines and FC. Wind turbines mostly find application in power generation for standalone RE system or microgrids. This is due to size and the dependence on wind speed/air density of the particular location. PV cells can serve microgrids, power satellites, communication equipment and specialised hybrid electric vehicles. FC has the advantage of portability. Hence it is suited for some hybrid electric vehicles and spacecrafts. Geothermal RE sources are not portable. This restricts them to provision of electricity for standalone and grid usage (Korompili and Monti, 2023).

Although unidirectional MICs are mostly used standalone RE power generation systems, some secondary power systems like ventilation of hybrid electric vehicles can use these MICs. For energy storage devices to exist in an MIC, there must be at least one bidirectional port in the MIC. In the bidirectional MICs, the most common storage devices are batteries, ultracapacitor and the supercapacitor. Battery banks are mostly used with PV, wind turbine and/or geothermal plant (Saadatizadeh et al., 2022).

**Table 2.1:** Renewable Energy Applications of Selected MICs

| Author | RE Source (s) | Industry Application |
|---|---|---|
| Ahrabi et al. (2017) | PV, FC, Battery | Hybrid Electric Vehicles |
| Kardan et al. (2017) | PV, FC, Battery | Standalone Power Generation |
| Aravind et al (2023) | PV, Ultracapacitor, Battery | Hybrid Electric Vehicles |
| Ghavidel et al. (2019) | PV, FC, Battery | RE Microgrid |
| Mahmoodieh & Deihimi (2019) | PV, FC, Wind, Battery | Smart grid connected with distributed generators |
| Alizadeh Asl et al. (2022a) | PV, FC, Battery | DC Motors |
| Alizadeh Asl et al. (2022b) | PV, FC, Wind, Battery | Standalone Power Generation |
| Athikkal & Eswar (2021) | PV, FC | Electric Vehicle Charging |
| Nnachi et al. (2023) | PV, FC | Data Centres |
| Harini et al. (2022) | PV, Grid | Electric Vehicle Charging |
| Shoaei et al. (2022) | PV | Dc Microgrid |

## 2.6 Review of Control Methods for RE Based MICs

In the scheme to control MICs which combine RE sources and battery storage, it is essential that the control method is stable and robust in order to maintain reliable and efficient operation. It is expected that the control method chosen, has an acceptable

smoothing effect and save cost. This review will focus on multivariable control methods since the existence of two or more switches in the MIC, mostly implies that there are two or more variables to be controlled.

### 2.6.1 PI/PID Control

The most common control method for RE based MICs is the application of PI control to the system. The PI controller is chosen mostly because of the simple implementation (Gorji et al., 2019). For a single loop control, the output of the controlled variable is fed to change the duty ratio of the switch. Some demerits of the PI controller are unsatisfactory dynamic response, poor reaction to disturbances and low capacity to handle varying operating points.

For multi-loop PI control, the major challenge faced is the coupling between the variables. The use of a decoupler has been proposed to prevent coupling between the variables. The decoupler is typically positioned between the output and the system input. The decoupler also maintains the stability of the system by tracking the variation in reference point, of the state variables.

Numerous types of decouplers have been found in the literature. For HRE based MICs, a decoupling network has been proposed. The decoupling network used in Nejabatkhah et al. (2012) was derived from the state space model after which an appropriate compensator was designed. A challenge faced by the decoupling network is the need for a complicated compensator.

### 2.6.2 Linear Quadratic Regulator (LQR) Control

The LQR is a type of optimal control method. In optimal control, a strategy to minimise the cost function is achieved by designing a control law that incorporates the state equations and the test conditions of the converter. The LQR method is widely applied and functions on a linearised converter model. The quadratic terms of the state vector and the control input are included in cost function. While the quadratic terms of the state vector minimise the average energy of the converter, the quadratic terms of the control input minimise the control effort (Korompili & Monti, 2023). The cost function, **J** (Brahimi et al., 2022) is defined by,

$$J = \int_0^\infty (x^T Q x + u^T R u) dt \qquad \text{Equation 2.1}$$

In Equation 2.1, *x* is the state vector and, *u* is the control input. Q and R represent the weighting matrices for the state vector and the input control respectively.

When applied in converter control, the steady-state gain is utilised. There is no need to store time-varying gains as the exclusive requirement are the constant gain amplifier. This makes the design and implementation uncomplicated. This control method provides good gain and transient response to the converter. The control method was found to be quite robust over a wide range of operation. The performance of the LQR controller with respect to the settling time and overshoots has been found to be better than that of the PI controller (Abdulla et al., 2015). However, linearisation of the system prior to control resulted in poor reaction to large signal disturbances. Another drawback of LQR control is that the entire state vector must be measured. This poses a problem as it is very difficult to measure the entire state vector in converter control.

### 2.6.3 Sliding Mode Control

Sliding mode control is a nonlinear control method proposed for controlling variable structure systems. The classification of DC-DC converters as variable structure systems is due to the premise that the configuration transforms between structures depending on the switching pulses applied to the control input (Korompili & Monti, 2023). The objective of this control method is to take and perpetuate the converter states on the switching surface. As a nonlinear controller, the major edge over others is the simplicity of implementation unlike other nonlinear strategies that involve complex implementation. Another advantage is that it delivers fast closed loop response and is robust against large-signal disturbances (Mumtaz et al., 2021). A structure of sliding mode control is presented in Figure 2.24.

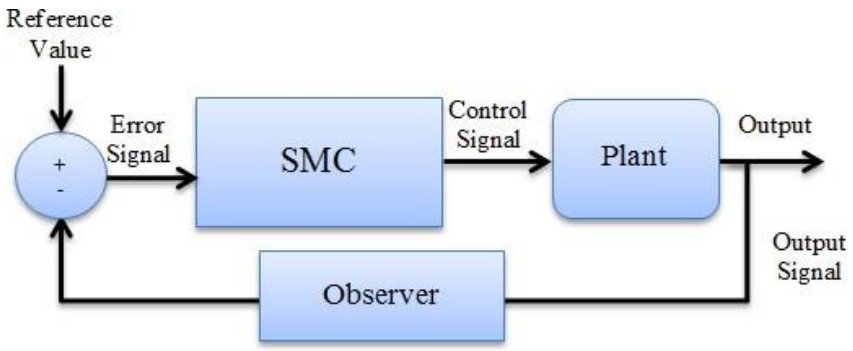


**Figure 2.24:** Sliding Mode Control (Mumtaz et al., 2021)

The primary drawback of sliding mode controller is that, it requires infinitely high switching frequencies in order to maintain the performance during the sliding stage. The variable frequency nature results in losses due to electromagnetic interference (EMI). The robustness exhibited against large-signal disturbances is absent when faced with mismatched disturbances (Korompili &Monti, 2023).

### 2.6.4 Artificial Neural Network Control

An artificial neural network (ANN) is an intelligence control that is inspired by the human biological nervous systems. The typical ANN model operates by a learning process. This makes the controller suitable for nonlinear control systems. There are numerous interconnected elements known as neurons, that work together to obtain required results (Chan et al.,1993). Each neuron encompasses a chunk of internal properties identified as weights. An illustration of the neural network control scheme is depicted in Figure 2.25.

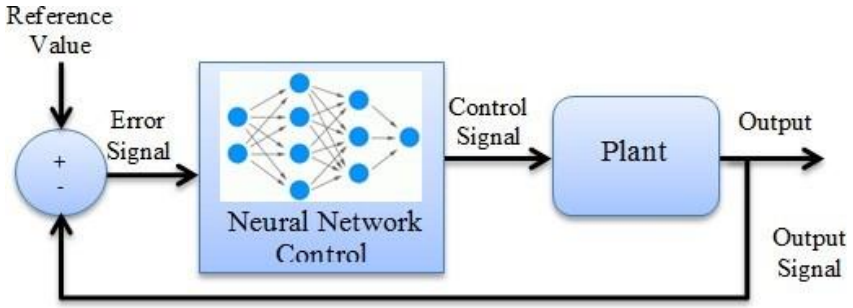


**Figure 2.25:** A Neural Network Control System (Chan et al.,1993)

The weights of the neurons are linked with the entire network. Thus, any alterations in the weights, impact on the performance of the neuron, as well as the action of the whole network. This implies that while training the ANN, the weights of all neurons are self-tuned to produce the relevant input-output relationship. The fact that the ANN do not need a comprehensive knowledge of the plant model to attain results is one merit of the scheme. In control of DC-DC converters, the ANN can apply its underlying ability to learn and reproduce highly nonlinear transfer functionality that permits efficient control to be accomplished efficiently for large-signal conditions (Leyva et al., 1997).

A backpropagation learning algorithm was developed in voltage tracking of a flyback converter (Utomo et al., 2011). The results showed an improved performance especially in

the voltage tracking response as compared to the conventional PI controller. The effectiveness of the control method is evident in decreased overshoot and reduced settling time.

Dhivya et al. (2013) used the ANN for a boost converter. The controller was able to achieve stabilisation for the output voltage while improving the performance during transient operations. The authors further highlighted the robustness of the proposed controller, regarding start up and reference voltage variations. Simulation of the ANN controller compared to the conventional PI controller showed an enhanced performance.

Khan et al. (2021) proposed the ANN control for a boost converter connected to DC microgrids. The authors obtained the training dataset via a model predictive control algorithm. The feed forward ANN was used in the study. Results showed a short settling time of the current waveform with little transients. Compared to the PI controller, the ANN showed lower distortion and superior wave quality.

## 2.7 Previous Research on HRE based Control of MICs

PID control of the multi-input single inductor boost converter has been implemented (Asadi et al., 2023). Two PID control schemes are cascaded and eliminated the use of a decoupling network. The converter has high robustness, no steady state errors and fast dynamics. The loss profile however showed relatively high losses via the inductor, switches and diodes. The PI control was applied to a two-input boost converter (Khwan-on & Kongkanjana, 2017). There are two inner loops that control the current of the two inductors. The outer control loop handles the voltage of the output capacitor.

A method of developing control system of MICs was proposed in Nejabatkhah et al. (2012). It involved calculating the decoupling network, on which basis the compensator would be designed. The issues faced by the control method included the complicated compensator design and a small range of stability.

Danyali et al. (2014) proposed the pole placement method. This method requires a sensor for even state variables that do not require control. Such requirement implies a very high cost of implementation. Also, the noise in the system becomes amplified using this method. The method proposed in Zhang et al. (2016) cannot be validated. The converter proposed by Kardan et al. (2017) did not investigate the control aspect. However, the absence of an input port delivering continuous current for the PV input posed a problem.

The decentralised control proposed by Zhao and Kwasinsky (2012) used the proportional and integral (PI) controllers on a multiple input SEPIC. The method requires sufficient loop pairing in order to reduce loop interactions. The converter experienced long transients due to the small bandwidth. Another decentralised control method focused on controlling a DC motor as load (Alizadeh Asl et al., 2022a). The authors were able to reduce the number of sensors while maintaining the reliability of the system. The PI controller used does not require a decoupling network. Linear quadratic optimal control method was used by Mahmoodieh and Deihimi (2019). This control method is quite systematic in obtaining the state-feedback control gain matrix (Deihimi & Mahmoodieh, 2017).

## 2.8 Identification of the Study Gap

Regarding the application of RE sources, the shortcomings which have earlier been highlighted have to be put into consideration in the choice of MICs. It is crucial to point out that different converter topologies have their best suited usage. Considering the electrically

connected MICs, the MICs that have provision for battery charging and discharge are recommended for RE applications.

A comparison of the converters with selected similar topologies has been conducted. All the converters compared, have a battery port and at least two other input ports. The initial comparison is done in terms of total number of components and voltage gain. The voltage boosting techniques applied in the converters have been identified. It should be noted that only the three-input version has been considered for the MIC proposed by Mahmoodieh and Deihimi (2019).

Kardan et al. (2017) boast of lower total component counts, and also exhibits a lower voltage gain. Also, Kardan et al. (2017) does not produce continuous input current that is necessary for PV ports. Although Mahmoodieh and Deihimi (2019) boasts of having a high voltage gain, the highest component count can also be attributed to it. Hence, the converter proposed by Mahmoodieh and Deihimi (2019) is cost prohibitive.

The converter proposed in Ghavidel et al. (2019) has the second highest parts count and the lowest voltage gain. This is in contrast to that of Alizadeh Asl et al. (2022b), that is tied with Kardan et al. (2017) for the fewest parts count but boasts of a high voltage gain. The converter proposed by Alizadeh Asl et al. (2022b) may suffer low efficiency due to the existence of a high number of passive elements (mainly resistors) and high voltage stress on the semiconductor devices.

Table 2.2 shows the comparisons between the research presented in this thesis and the work of other researchers on configuration circuit for thee input converters with an integrated battery port. The gap of study can easily be identified from the comparison. No researchers have investigated the three-input DC-DC converter with the non-coupled

inductor / boost topology. The complexities associated with decoupling higher order multivariable systems make the ANN to be chosen as the control method. Simulation will be done using the MATLAB/Simulink platform while the dSPACE DS1104 real-time digital controller board will be used to generate the switching signals during experimentation on a laboratory prototype.

**Table 2.2:** Study Gap from Previous Research on HRE based MICs

| Author | Configuration circuit | Inductor Count | Control Method |
|---|---|---|---|
| Ahrabi et al. (2017) | Double Boost | 2 | PI controller |
| Kardan et al. (2017) | Buck-boost/ Boost | 2 | - |
| AboReada et al. (2019) | Boost/ Buck | 3 | - |
| Ghavidel et al. (2019) | Switched Capacitor Inductor/ Boost | 5 | - |
| Mahmoodieh & Deihimi (2019) | Switched inductor | 4 | LQR optimal control |
| Alizadeh Asl et al. (2022a) | Double Buck-boost | 2 | - |
| Alizadeh Asl et al. (2022b) | Boost / Boost | 2 | Decentralised PI controller |
| Proposed by Azuka Affam | Boost/Non-Coupled Inductor | 3 | ANN |

## 2.9 Summary

In summary, magnetically and electromagnetically connected MICs are bulky and heavy. They require conversion of DC to AC and AC to DC on either side of the isolating transformer. This implies additional circuitry and devices. Also, while they can deliver high

voltage gain based on the transformer turns ratio, a complicated gate drive circuit and a controller are needed, thereby incurring high cost for the converter.

Electrically connected MICs are compact in design. They have lower semiconductor current stress, no limitation for switching duty cycle, better efficiency, simple structure, and lower cost. Additionally, there is high pliability for the output voltage and wide control range of the different input ports. These make them suitable in both low and high power HRES.

# CHAPTER 3

# MATERIALS AND METHODS

## 3.1 Overview

In this chapter, the proposed BITIHGC will be presented and discussed. In designing the converter, the RE sources, energy storage options, operation modes, switching patterns, and component selection are areas that deserve great attention. The energy management and control schemes are also presented.

## 3.2 Research Flowchart

The research flowchart is presented in Figure 3.1. The first step was to identify the scenarios that can arise when RE sources are used in providing power. Such scenarios depend on the availability and power level of the RE sources. This leads to the determination of the respective operation modes that the proposed converter possesses. The next step encompassed developing the converter configuration and assigning the switching patterns. In doing this, the switching period was taken into consideration.

The success of the first two steps meant that the next step was the steady state analyses and dynamic modelling of the proposed converter. Here, the output voltage equations were obtained for the chosen operation modes. In addition, the small signal modelling of the converter was gone for all the modes. Other necessary analyses were also performed. The design of the energy management algorithm followed the successful analyses after which the neural network control was developed and trained.

The simulation of the proposed circuit using MATLAB Simulink, development of the hardware and the integration of the software with hardware follow in quick succession.

Thereafter, validatory experiments were conducted using the integrated hardware and software. The research process culminated in the compilation and analyses of the obtained results.

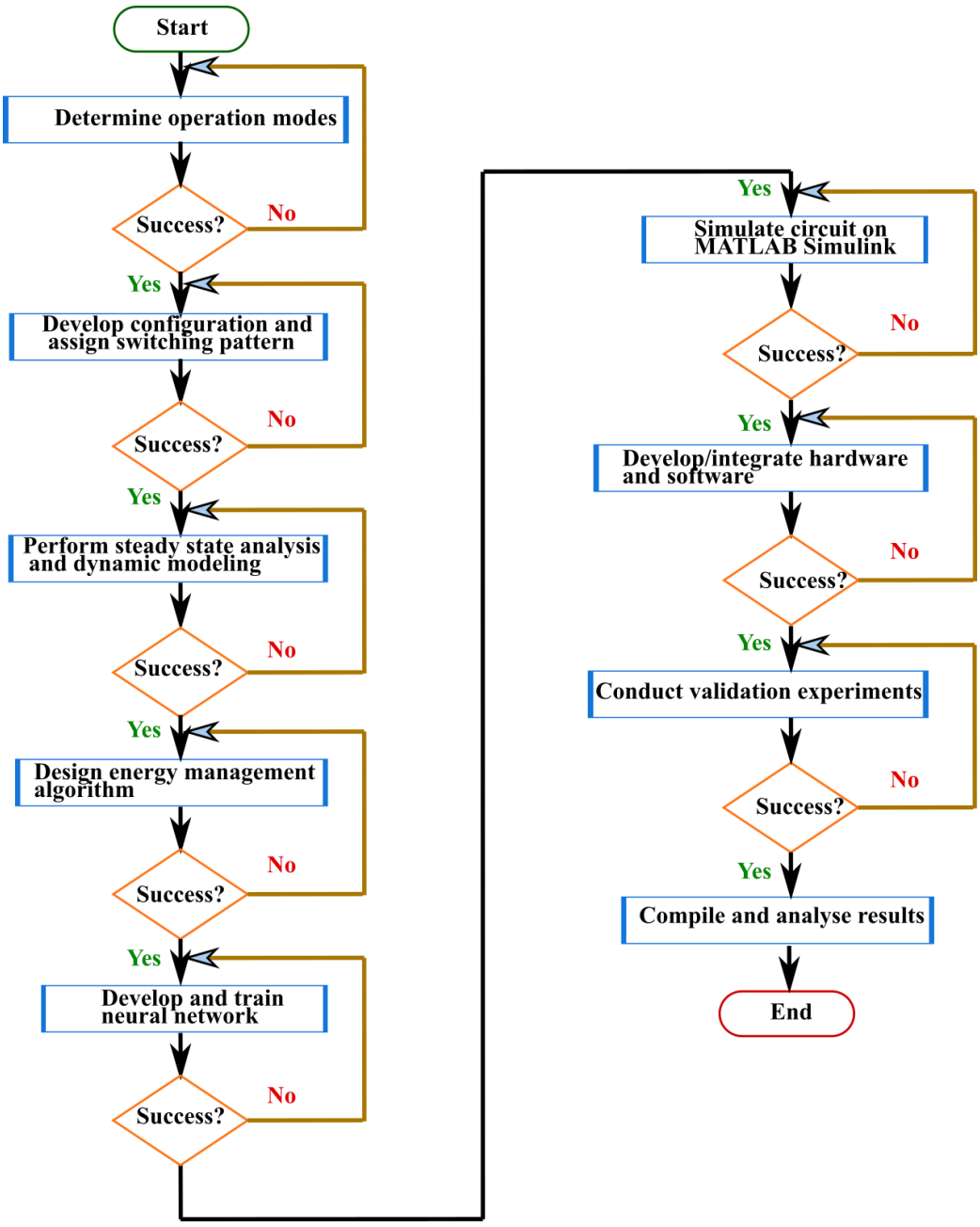


**Figure 3.1:** Research Flowchart

## 3.3 Operation Modes of the Proposed Converter

The fluctuation of RE sources implies that efforts should be geared toward maintaining a considerable stability in output voltage supply to the load irrespective of the input voltage levels. It is envisaged that three scenarios could arise in the course of serving the load. These scenarios are discussed subsequently.

### 3.3.1 Operation Mode One (Battery Bypassing Mode)

The first scenario is one where the two RE sources are able to satisfy the load requirement. In this scenario, the fully charged battery is not required to contribute to the input voltage levels. This is the default operation mode that proposed BITIHGC should operate in. This situation requires that the battery supply is cut off using a power switch. Battery charging should also be disabled during this mode. The operation and switching will be further explained in subchapter 3.6.1.

### 3.3.2 Operation Mode Two (Battery Discharging Mode)

A scenario could arise when either or both of the RE sources have dipped in voltage levels, or have become unavailable. Such a situation may lead to inability to serve the load. At this point, it becomes imperative to call in the battery supply to the converter. Hence, the battery power supplements that of the RE sources. The operation and switching will be further explained in subchapter 3.6.2.

### 3.3.3 Operation Mode Three (Battery Charging Mode)

When the both of the RE sources are at optimal voltage/ power levels, and the battery supply is depleted, the third scenario arises. The battery needs to be charged with the BITIHGC still delivering power to the load. This could also happen when there is a lower

load demand alongside a depleted battery storage. The operation and switching will be further explained in subchapter 3.6.3.

## 3.4 Configuration of the Proposed BITIHGC

The proposed BITIHGC is designed to integrate two different RE sources and a battery storage. This would provide redundance to the system during periods of unavailability of either energy source. The addition of battery storage increments the number of input sources to three. Figure 3.2 shows the block diagram of the proposed BITIHGC. There are two converter cells. Each of the two main energy sources are assigned to a converter. The storage unit is inserted between the energy sources. The storage unit is positioned such that it can support either of the energy sources, and can also be fed by the energy sources.

### 3.4.1 Boost Converter Circuit

In this part of the converter, energy source, $V_1$ is assigned to the traditional boost converter. Switch, $S_1$ serves to charge or discharge the inductor, $L_1$ which functions as the buffer stage. The capacitor, $C_1$ is positioned before the output diode. The circuit is shown in Figure 3.3. The output diode, $D_1$ and output capacitor, $C_o$ complete the circuit.

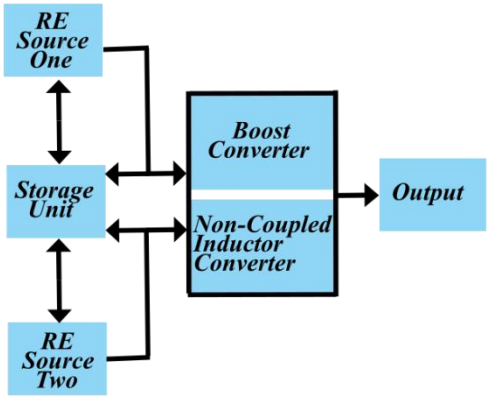


**Figure 3.2:** Block Diagram of the Proposed BITIHGC

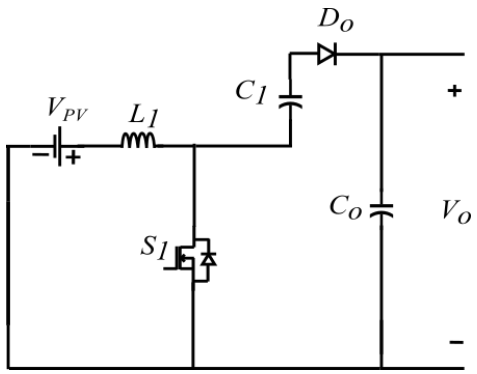


**Figure 3.3:** Boost Converter Block of the Proposed BITIHGC

### 3.4.2 Non-Coupled Inductor Boost Converter Circuit

In this part of the converter, the second energy source, $V_2$ is tied to the non-coupled inductor boost converter. Figure 3.4 shows the non-coupled inductor circuit when it is operated in a standalone mode. The non-coupled inductor side consists of power switch, $S_2$, Inductors, $L_2$ and $L_3$, diode, $D_m$, and capacitors, $C_2$ and $C_3$. $D_1$ and $D_o$ are series connected and form the output diode. The components, $L_3$, $D_m$, $C_2$ and $C_3$ help to improve the voltage gain of the converter. Inductor $L_3$ serves as an extra energy buffer, diode $D_m$ serves as a free-

wheeling diode, while capacitors, $C_2$ and $C_3$ charge alternately to ensure higher steady charge to either inductor, $L_3$ or the load.

### 3.4.3 Battery Storage Circuitry

The battery circuit is shown in Figure 3.5. Switch, $S_3$ is positioned in series with diode, $D_{b2}$. This same series connection is done for switch, $S_4$ and diode, $D_{b1}$. The battery is placed in between to form a parallel connection with both switch/diode pairs. It should be noted that $S_3$ and $D_{b4}$ are the topmost components in their respective switch/ diode pairs.

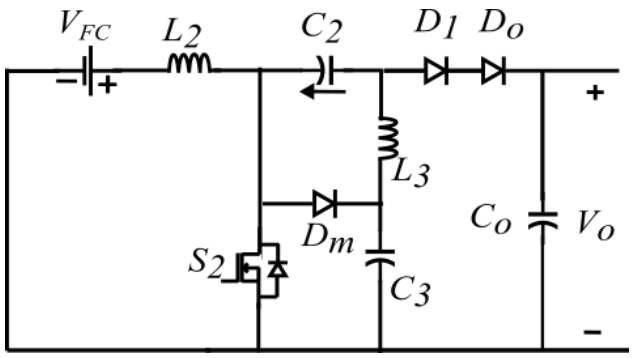


**Figure 3.4:** Non-Coupled Inductor Block of the Proposed BITIHGC

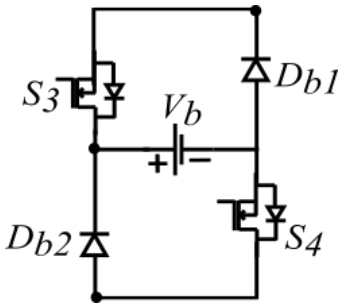


**Figure 3.5:** Battery Charging and Discharge Block of the Proposed BITIHGC

## 3.5 Switching Patterns for Proposed converter

During the development of MICs, the switching patterns are adopted with the objective of having the energy sources deliver power to the load individually or

simultaneously. In event of failure of one side of the converter, the other side should be able to satisfy the load. The total period has been divided into four switching states. The switching pattern for operation mode one is presented in Figure 3.6. *T* is the total switching period. Figure 3.7 shows the switching pattern for operation mode two, while Figure 3.8 shows the switching pattern for operation mode three. The switching patterns are the same for switches, $S_1$ and $S_2$, in all the operation modes but vary for switches, $S_3$ and $S_4$ in the different operation modes.

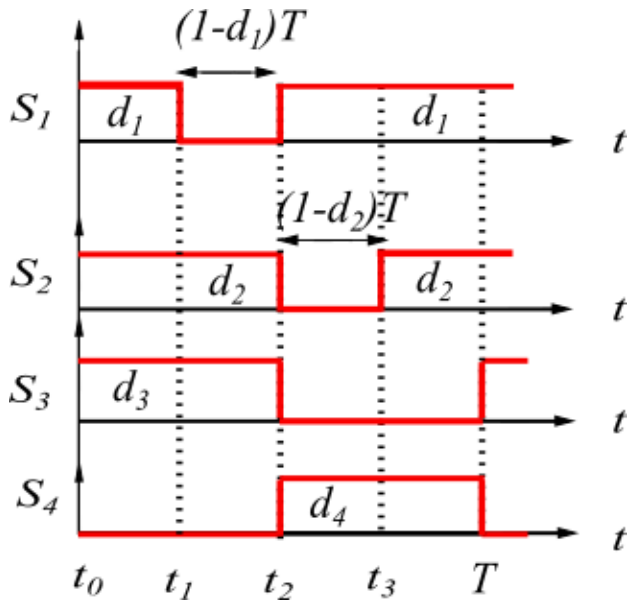


**Figure 3.6:** Switching Pattern for Operation Mode One

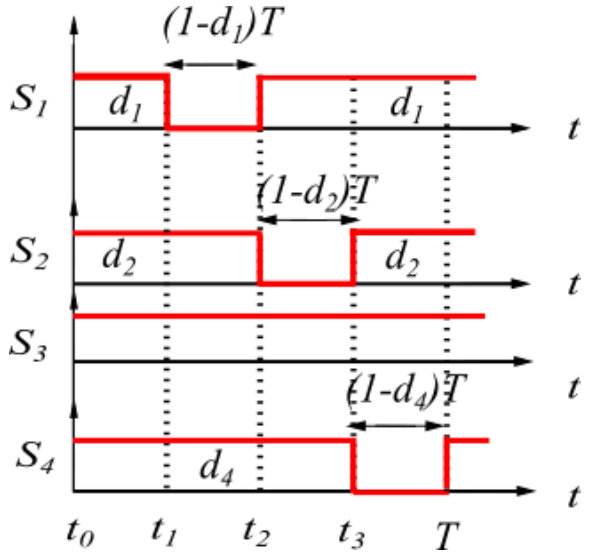


**Figure 3.7:** Switching Pattern for Operation Mode Two

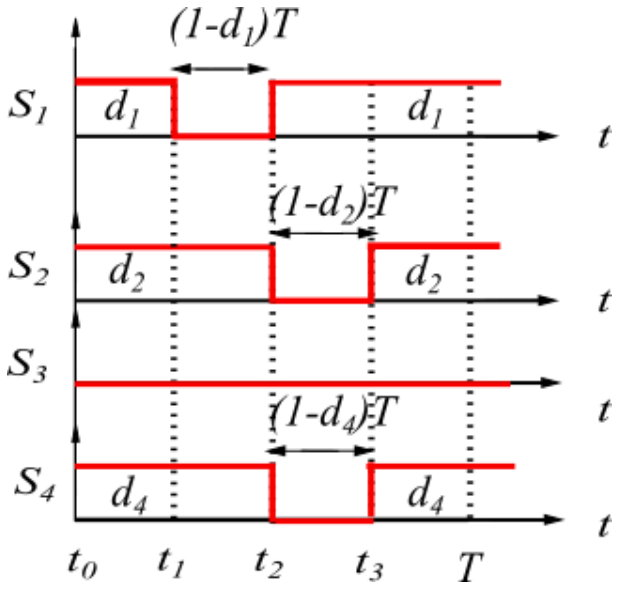


**Figure 3.8:** Switching Pattern for Operation Mode Three

## 3.6 Operating Principle of Proposed Converter

The combined circuit of the proposed converter is shown in Figure 3.9. The right side of this converter is a conventional boost converter. On the left side is the non-coupled

inductor-based converter configuration. There are three inputs that can be identified as $V_1$, $V_2$ and $V_b$. $V_1$ is tied to the simple boost converter, $V_2$ serves the non-coupled inductor-based converter. $V_b$ is a battery source sandwiched between the two component converters. There are four power switches, $S_1$, $S_2$, $S_3$ and $S_4$ in the circuit. Switches, $S_1$ and $S_2$ serve the conventional boost converter and the non-coupled inductor-based boost converter respectively. Switches $S_3$ and $S_4$ serve to charge or discharge the battery as well as complete the flow of current. Other components of the converter include three inductors ($L_1$, $L_2$, $L_3$), five diodes ($D_o$, $D_1$, $D_{b1}$, $D_{b2}$, $D_m$), and four capacitors ($C_o$, $C_1$, $C_2$, $C_3$).

The switching patterns and waveforms for the inductor currents, and capacitor voltages are depicted in Figure 3.10. The operation for the respective operation modes and switching states are presented hereafter.

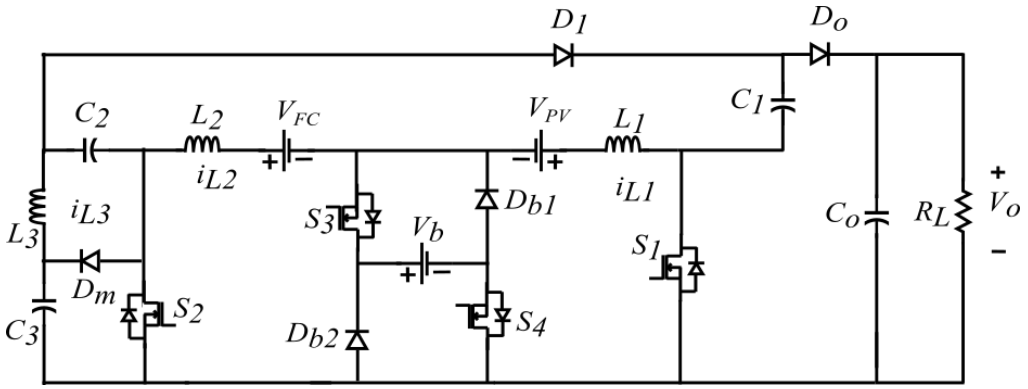


**Figure 3.9:** Schematic of the Proposed BITIHGC

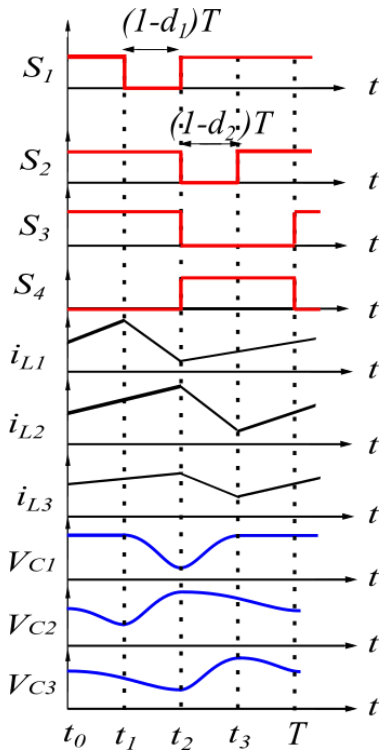


**Figure 3.10:** Waveforms of Inductor Currents and Capacitor Voltages

### 3.6.1 Switching States for Operation Mode One

As mentioned earlier, the first mode occurs when the supply power for $V_1$ and $V_2$ can satisfy the existing load. This mode of operation involves four switching states. Also at this

point, the battery is fully charged. The battery is cut off by turning off either pair of $S_4$ and $D_{b1}$ or $S_3$ and $D_{b2}$. The switching states are described.

Switching state 1 ($t_0 - t_1$): During this switching state, switches $S_1$, $S_2$ and $S_3$ are turned on while $S_4$ is turned off. Diode, $D_{b1}$ does not conduct and cuts off supply to the battery. Figure 3.11 shows the circuit. Inductor $L_1$ is charged by input source $V_1$ through $S_1$. Similarly, $L_2$ is charged by $V_2$ through $S_2$. $C_3$ discharges to $L_3$ and $C_2$. $C_1$ is in idle state. $C_o$ serves the load during this switching state. $D_o$, $D_1$, and $D_m$ do not conduct.

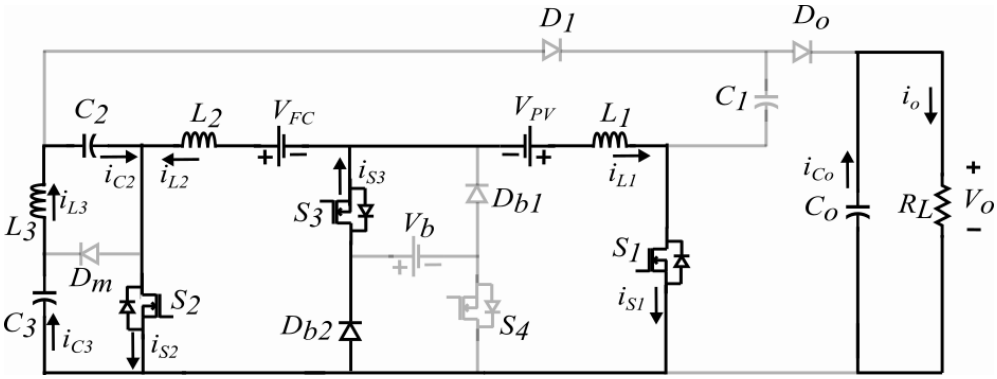


**Figure 3.11:** Current Path for Switching State 1 of Operation Mode One at time $t_0 - t_1$

The inductor current equations obtainable in this switching state are;

$$\frac{di_{L1}}{dt} = \frac{V_1}{L_1} \qquad \text{Equation 3.1}$$

$$\frac{di_{L2}}{dt} = \frac{V_2}{L_2} \qquad \text{Equation 3.2}$$

$$\frac{di_{L3}}{dt} = \frac{V_{C3} - V_{C2}}{L_3} \qquad \text{Equation 3.3}$$

Switching state 2 ($t_1 - t_2$): The circuit is illustrated in Figure 3.12. During this state, Switches $S_1$ and $S_4$ are turned off while $S_2$ and $S_3$ are turned on. The state of the non-coupled inductor side of the converter remains the same. $D_o$ is forward bias hence $L_1$ and $C_1$ discharge in consonance with $V_1$ to deliver energy to the load.

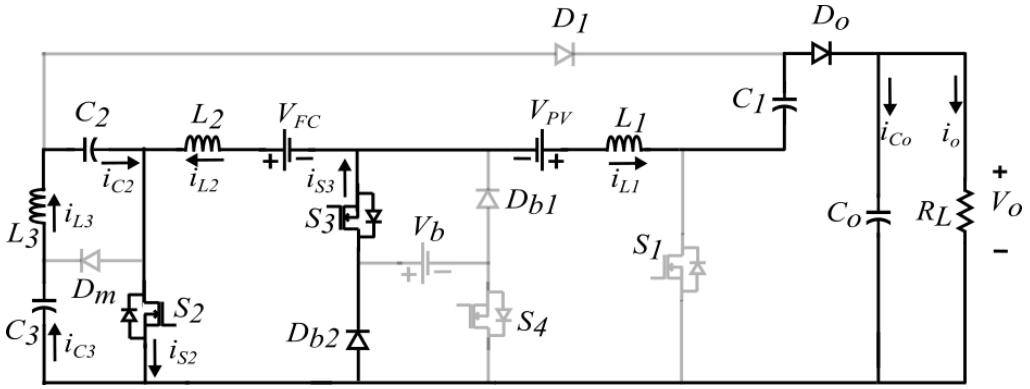


**Figure 3.12:** Current Path for Switching State 2 of Operation Mode One at time $t_1 - t_2$

The inductor current equations for $L_2$ and $L_3$ are given by Equation 3.2 and Equation 3.3 respectively.

$$\frac{di_{L1}}{dt} = \frac{V_1 + V_{C1} - V_o}{L_1} \qquad \text{Equation 3.4}$$

Switching state 3 ($t_2 - t_3$): The circuit is as shown in Figure 3.13. $S_1$ and $S_4$ are turned on while $S_2$ and $S_3$ are turned off. $S_4$ turns on to complete the circuit with $D_{b1}$. $D_o$ is turned off while $D_1$ and $D_m$ conduct. $L_1$ is charged by $V_1$. $C_3$ is charged by $V_2$ and $L_2$ through $D_m$. $L_3$ charges $C_1$ through $D_1$ and $C_o$ serves the load.

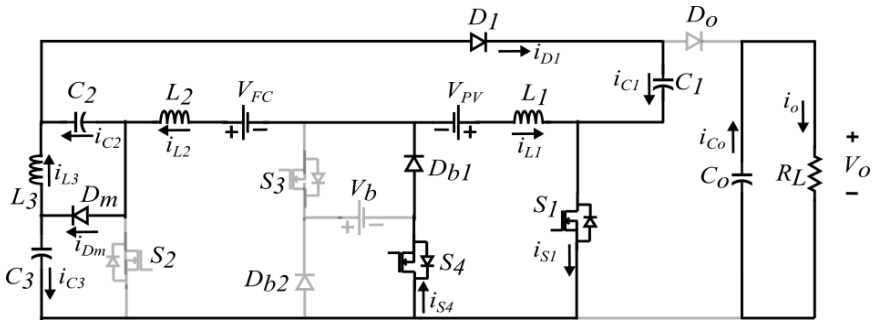


**Figure 3.13:** Current Path for Switching State 3 of Operation Mode One at time $t_2 - t_3$

The inductor current equation for $L_1$ is represented by Equation 3.1. Other equations obtainable during this switching state are;

$$\frac{di_{L2}}{dt} = \frac{V_2 + V_{C2} - V_{C1}}{L_2} \qquad \text{Equation 3.5}$$

$$\frac{di_{L3}}{dt} = \frac{-V_{C1}}{L_2} \qquad \text{Equation 3.6}$$

It can be observed from Figure 3.12 that inductor, $L_2$ formed two loops. One loop where capacitor, $C_1$ is charged and another loop where capacitor, $C_3$ is charged. Equation 3.5 represents the expression for the loop where $C_1$ is charging. The expression for $C_3$ charging loop is given by;

$$\frac{di_{L2}}{dt} = \frac{V_2 - V_{C3}}{L_2} \qquad \text{Equation 3.7}$$

Switching state 4 ($t_3 - T$): $S_1$, $S_2$, and $S_3$ are turned on. $D_o$ is turned off. The components exhibit the same pattern as in switching state 1. $C_o$ serves the load.

### 3.6.2 Switching States for Operation Mode Two

In this operation mode, the load cannot be served by the RE sources alone. Hence, the battery storage, $V_b$ is engaged to support the power delivered to the load. Switches $S_3$ and $S_4$ play the role of allowing or disallowing the battery to deliver power to the load. $S_3$ is perpetually turned on during this operation mode. The respective switching states are described hereafter.

Switching state 1 ($t_0 - t_1$): The circuit is represented in Figure 3.14. Switches, $S_1$, $S_2$, $S_3$ and, $S_4$ are turned on. Diodes, $D_{b1}$ and $D_{b2}$ are turned off. The battery, $V_b$ forms a series connection with $V_1$ and $V_2$ thus complementing them to charge inductors $L_1$ and $L_2$. Capacitor, $C_1$ is idle. $D_o$ and $D_1$ are reverse biased. $C_o$ delivers power to the load.

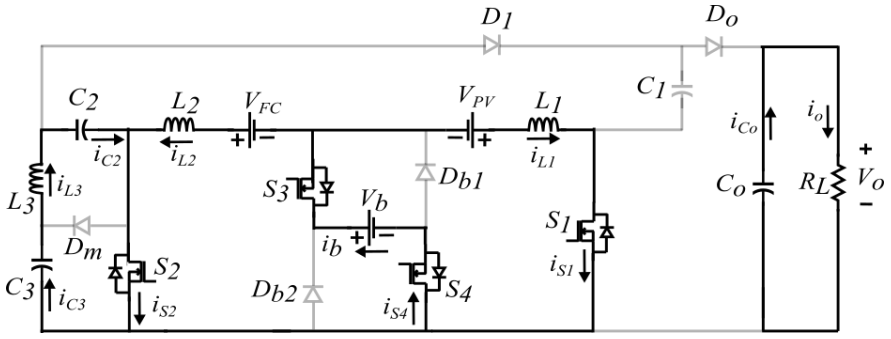


**Figure 3.14:** Current Path for Switching State 1 of Operation Mode Two at time $t_0 - t_1$

Equation 3.3 gives the change in inductor current equation for $L_3$. Other equations obtainable in this switching state are;

$$\frac{di_{L1}}{dt} = \frac{V_1 + V_b}{L_1} \qquad \text{Equation 3.8}$$

$$\frac{di_{L2}}{dt} = \frac{V_2 + V_b}{L_2}$$ Equation 3.9

Switching state 2 ($t_1 - t_2$): The equivalent circuit is shown in Figure 3.15. Switches, $S_2$, $S_3$ and $S_4$ are turned on while $S_1$ is turned off. The non-coupled inductor side of the converter remains in the same state as the previous switching state. However, battery, $V_b$ supplies power to the load via the series connection with $V_1$, $C_1$ and $D_o$.

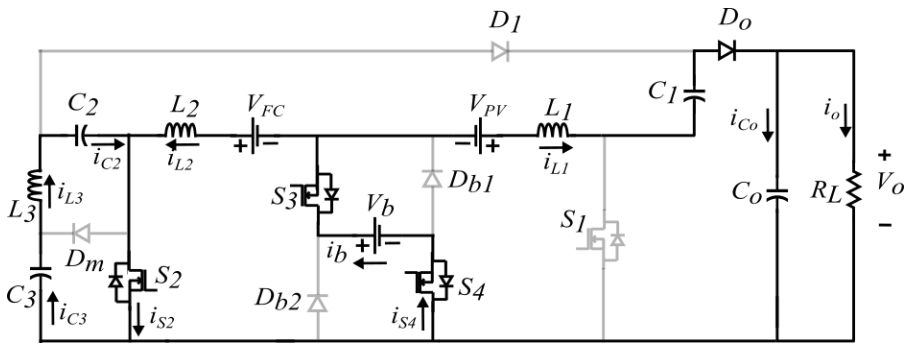


**Figure 3.15:** Current Path for Switching State 2 of Operation Mode Two at time $t_1 - t_2$

$$\frac{di_{L1}}{dt} = \frac{V_1 + V_b + V_{C1} - V_o}{L_1}$$ Equation 3.10

Switching state 3 ($t_2 - t_3$): The circuit is shown in Figure 3.16. Switches, $S_1$, $S_3$ and $S_4$ are turned on, thereby enabling $V_b$ to charge $L_1$ and $L_2$. $S_2$ is turned off. $C_o$ serves the load.

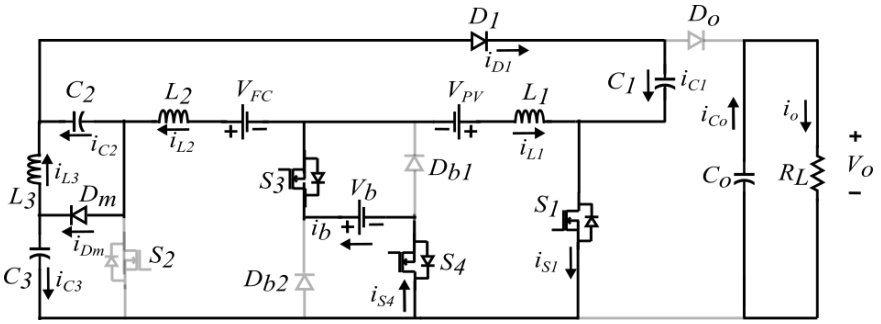


**Figure 3.16:** Current Path for Switching State 3 of Operation Mode Two at time $t_2 - t_3$

$$\frac{di_{L2}}{dt} = \frac{V_2 + V_b + V_{C2} - V_{C1}}{L_2} \quad \text{Equation 3.11}$$

$$\frac{di_{L3}}{dt} = \frac{-V_{C1}}{L_3} \quad \text{Equation 3.12}$$

$$\frac{di_{L2}}{dt} = \frac{V_2 + V_b - V_{C3}}{L_2} \quad \text{Equation 3.13}$$

Switching state 4 ($t_3 - T$): $S_1$, $S_2$ and $S_3$ are turned on while $S_4$ is turned off. Hence switching state 4 of operation mode one is replicated here.

Since the battery is discharged during this operation mode, the battery current, $i_b$ and battery power, $P_b$ can be expressed as;

$$i_b = i_{L1} + i_{L2} \quad \text{Equation 3.14}$$

$$P_b = V_b(i_{L1} + i_{L2}) \quad \text{Equation 3.15}$$

### 3.6.3 Switching States for Operation Mode Three

In this operation mode, the battery *SOC* is low and the RE sources have the capacity to charge the battery while serving the load. Switch $S_4$ regulates the charging of the battery. $S_3$ is turned off during this operation mode. The switching modes are described.

Switching state 1 ($t_0 - t_1$): Switching state 1 of operation mode one is replicated here. Switch $S_4$ is turned on hence the battery is not charging.

Switching state 2 ($t_1 - t_2$): Switching state 2 of operation mode one is repeated here. Switches, $S_2$ and $S_3$ stay on. The other switches are turned off. $L_2$ is continues charging by $V_2$. $D_o$ is forward bias hence $L_1$ and $C_1$ discharge to the load. The battery does not charge during this switching state.

Switching state 3 ($t_2 - t_3$): The circuit is shown in Figure 3.17. Switch, $S_2$, is turned on while $S_1$, $S_3$ and $S_4$ are turned off. $D_{b1}$ and $D_{b2}$ conduct. $V_b$ is charged along with $C_3$ by both $V_1$, $V_2$, and energy discharged from $L_2$. $C_o$ deliver power to the load.

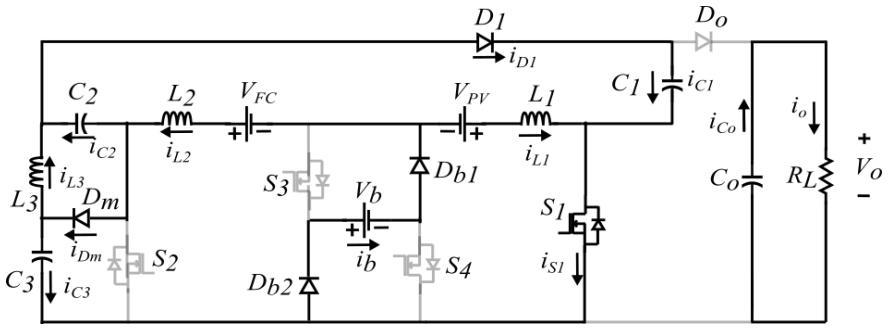


**Figure 3.17:** Current Path for Switching State 3 of Operation Mode Three at time $t_2 - t_3$

$$\frac{di_{L1}}{dt} = \frac{V_1 - V_b}{L_1} \qquad \text{Equation 3.16}$$

$$\frac{di_{L2}}{dt} = \frac{V_2 - V_{C3} - V_b}{L_2} \qquad \text{Equation 3.17}$$

Switching state 4 ($t_3 - T$): $S_1$, $S_2$ and $S_3$ are turned on while $S_4$ is turned off. This switching mode is the same as the switching state 1 of the first operation mode. No charging current enters the battery.

Since the battery is charged during this operation mode, the battery current, $i_b$ and battery power, $P_b$ can be expressed as;

$$i_b = i_{L1} + i_{L2} + i_{L3} \qquad \text{Equation 3.18}$$

$$P_b = V_b(i_{L1} + i_{L2} + i_{L3})) \qquad \text{Equation 3.19}$$

## 3.7 Output Voltage and Voltage Gain of Proposed Converter

The description of the operation modes of the proposed converter under CCM has been done in steady-state conditions. For analysis, it is assumed that all components are ideal. Also, the capacitances of the capacitors are large such that their voltage levels are viewed as constant during the entire time period.

### 3.7.1 Output Voltage and Voltage Gain for Operation Mode One

During this operation mode, the duty ratios of switches, $S_1$ and $S_2$, are $d_1$ and $d_2$ respectively. The volt-second balance theory states that, the average inductor voltage over a single switching period should be zero. Thus, applying this theory,

$\int_0^T v_L = L\frac{di_L}{dt} = 0$ (Mohan et al., 2003) Equation 3.20

Considering $L_1$ and $L_2$, the steady-state equations are

$$V_2 d_2 T_s - (1 - d_2)(V_2 - V_{C3})T_s = 0 \quad \text{Equation 3.21}$$

$$V_2 d_2 T_s + (1 - d_2)(V_2 + V_{C2} - V_{C1})T_s = 0 \quad \text{Equation 3.22}$$

$$V_1 d_1 T_s + (1 - d_1)(V_1 + V_{C1} - V_o)T_s = 0 \quad \text{Equation 3.23}$$

Solving Equation 3.21, the voltage on capacitor, $C_3$ can be expressed as

$$V_{C3} = \frac{2V_2}{1 - d_2} \quad \text{Equation 3.24}$$

Similarly, Equation 3.22 can be manipulated to obtain the voltage on capacitors $C_2$ and $C_1$.

$$V_{C2} = \frac{3V_2}{2 - 2d_2}$$ Equation 3.25

$$V_{C1} = V_{C2} + V_{C3} = \frac{7V_2}{2 - 2d_2}$$ Equation 3.26

The output voltage for this first operation mode can be obtained by solving Equation 3.23 as shown in Equation 3.26.

$$V_o = \frac{V_1 + V_{C1}(1 - d_1)}{1 - d_1}$$ Equation 3.27

$$V_o = \frac{V_1 + ((\frac{3V_2}{2 - 2d_2} + \frac{2V_2}{1 - d_2})(1 - d_1))}{1 - d_1}$$ Equation 3.28

In order to derive the expression for the voltage gain, a scaling factor, *k* is applied, such that we have, $V_1 = kV$ and $V_2 = V$. we can express the output voltage of the first operation mode, $V_o$ as

$$V_o = \frac{kV + V(\frac{3}{2 - 2d_2} + \frac{2}{1 - d_2}(1 - d_1))}{1 - d_1}$$ Equation 3.29

If $V_1 = V_2 = V$ and $d_1 = d_2 = d$, we have that,

$$V_o = \frac{V(1 + (\frac{3}{2 - 2d} + \frac{2}{1 - d}(1 - d))}{1 - d}$$ Equation 3.30

Hence, the voltage gain in the first operation mode is,

$$G_{Vmode1} = \frac{V_o}{V} = \frac{9}{2(1 - d)}$$ Equation 3.31

Substituting $d$ = 75 % in Equation 3.29, a voltage gain of 18 is obtained for the first operation mode.

### 3.7.2 Output Voltage and Voltage Gain for Operation Mode Two

In this operation mode, the applied duty ratios are $d_1$, $d_2$ and $d_4$ emanating from $S_1$, $S_2$ and $S_4$ respectively. While still applying the voltage-second balancing rule, the following steady-state equations can be obtained.

$$V_2 d_2 T_s + V_b d_4 T_s - V_2 + V_b d_4 - V_{C3}(1 - d_2) T_s = 0 \quad \text{Equation 3.32}$$

$$V_2 d_2 T_s + V_b d_4 T_s + V_b d_4 + V_2 + V_{C2} - V_{C1}(1 - d_2) T_s = 0 \quad \text{Equation 3.33}$$

$$V_1 d_1 T_s + V_b d_4 - V_b d_4 + V_1 + V_{C1} - V_o(1 - d_1) T_s = 0 \quad \text{Equation 3.34}$$

Manipulating the equations as done in the first operation mode, the voltage expressions can be obtained.

$$V_{C3} = \frac{V_b(1 + d_4) + V_2(1 + d_2)}{1 - d_2} \quad \text{Equation 3.35}$$

$$V_{C2} = \frac{V_2(2 + d_2) + V_b(2 - d_2 + 2d_4)}{2 - 2d_2} \quad \text{Equation 3.36}$$

$$V_{C1} = \frac{V_b(1 + d_4) + V_2(1 + d_2)}{1 - d_2} + \frac{V_2(2 + d_2) + V_b(2 - d_2 + 2d_4)}{2 - 2d_2} \quad \text{Equation 3.37}$$

$$V_o = \frac{V_1 + (V_b(1 - d_1 + d_4)) + (V_{C1}(1 - d_1))}{1 - d_1} \quad \text{Equation 3.38}$$

If $V_1 = V_2 = V_b = V$ and $d_1 = d_2 = d_4 = d$, the voltage gain in the second operation mode can be expressed as,

$$G_{Vmode2} = \frac{V_o}{V} = \frac{4 + 3d}{1 - d} \quad \text{Equation 3.39}$$

### 3.7.3 Output Voltage and Voltage Gain for Operation Mode Three

The duty ratios, $d_1$, $d_2$ and $d_4$ control the output voltage during this operation mode. The steady-state equations are obtained as.

$$V_2 d_2 T_s - (V_2 - V_{C3} - V_b(1 - d_4))(1 - d_2)T_s = 0 \quad \text{Equation 3.40}$$

$$V_2 d_2 T_s + V_2 + V_{C2} - V_{C1}(1 - d_2)T_s = 0 \quad \text{Equation 3.41}$$

$$V_1 d_1 T_s - V_b(d_1 - d_4) - V_1 + V_{C1} - V_o(1 - d_1)T_s = 0 \quad \text{Equation 3.42}$$

The voltage expressions are therefore obtained as

$$V_{C3} = \frac{V_2 + V_b(1 - d_2 + d_4 + d_2 d_4)}{1 - d_2} \quad \text{Equation 3.43}$$

$$V_{C2} = \frac{V_2 + V_{C3}(1 - d_2)}{2 - 2d_2} \quad \text{Equation 3.44}$$

$$V_{C1} = \frac{V_2 + \frac{V_2 + V_b(1 - d_2 + d_4 + d_2 d_4)}{1 - d_2}}{2 - 2d_2} + \frac{V_2 + V_b(1 - d_2 + d_4 + d_4 d_2)}{1 - d_2} \quad \text{Equation 3.45}$$

$$V_o = \frac{V_1 + (V_b(d_1 - d_4)) + ((V_{C1}(1 - d_1))}{1 - d_1} \quad \text{Equation 3.46}$$

If $V_1 = V_2 = V_b = V$ and $d_1 = d_2 = d_4 = d$, the voltage gain in the second operation mode can be expressed as,

$$G_{Vmode3} = \frac{3 + 3d^2 - 2d - 2d^3}{2(1 - d)} \quad \text{Equation 3.47}$$

## 3.8 Component Selection of the Proposed Converter

After perusing the architecture of the proposed BITIHGC, the components that require selection, design and justification can be identified. The inductors, capacitors,

switches and diodes are the main components that must be designed to meet the specifications of the converter. For the input voltage sources, $V_1$ = 6 *V*, $V_2$ = 12 *V*, $V_b$ =12 *V*, duty ratios, $d_1 = d_4$ = 75 %, and $d_2$ = 70 %, $d_3$ = 50 %. The parameters are obtained from operation mode two are used for component design because, in this operation mode, there is more tendency for the current to operate in DCM. After substituting the chosen parameters in in the equations, the values for the output voltage and voltage of the capacitors can be obtained. These values will be used to determine the inductors and capacitors' values. The targeted ripple of the output current is 10 % while the selected output voltage ripple is 0.1 %. The frequency is tagged at 15 *kHz*.

### 3.8.1 Design of Inductors

The inductor design for the proposed converter is akin to the conventional boost converter. To achieve CCM, the inductor average current must be greater than half of the inductor ripple current. Hence, for an inductor *L*, the minimum inductor current, $I_L$ is given by

$$I_{L(min)} = I_L - \frac{\Delta i_L}{2} \text{ (Mohan et al., 2003)} \qquad \text{Equation 3.48}$$

Considering the equivalent circuits during operation mode two, the change in current for inductor, $L_1$ can be obtained as

$$\Delta i_{L1} = \frac{d_1 V_1 + d_4 V_b}{L_1 f_s} \qquad \text{Equation 3.49}$$

Similarly, for inductor, $L_2$, the change in current can be obtained as

$$\Delta i_{L2} = \frac{d_2 V_2 + d_4 V_b}{L_2 f_s} \qquad \text{Equation 3.50}$$

Manipulating Equation 3.49, the value of the inductance for an assumed ripple current is

$$L_{1min} = \frac{d_1 V_1 + d_4 V_b (1 - d_1)^2 R}{4 \Delta i_{L1} f_s} \quad \text{Equation 3.51}$$

For the non-coupled inductors, $L_2$ is identical to $L_3$. Hence the minimum inductance for the assumed ripple current is

$$L_{2min} \equiv L_{3min} = \frac{d_1 V_1 + d_4 V_b (1 - d_2)^2 R d_1}{4 \Delta i_{L2} f_s} \quad \text{Equation 3.52}$$

Adopting a ripple requirement of 10 % for the inductors, the minimum inductor value of 300.6 *mH* was obtained for inductor, $L_1$, while the minimum inductance of 157.3 *mH* was obtained for $L_2$ and $L_3$.

### 3.8.2 Design of the Capacitors

The function of capacitor, $C_o$ is to limit the output voltage ripple of the load. The parameters at play for the output filter are the load resistance, the duty ratio, the frequency, output voltage and the output voltage ripple. The capacitance of the output capacitor, $C_o$ can be expressed by

$$C_o \geq \frac{V_o d_1}{R f_s \Delta V_o} \quad \text{Equation 3.53}$$

For the output capacitor, 0.1 % output voltage ripple is allowed. Hence the value of the output capacitor was obtained as 50 $\mu F$.

For other capacitors in the converter, the allowable voltage ripple was 1 %. For the capacitor, $C_1$, the capacitance can be expressed as

$$C_1 \geq \frac{V_o}{Rf_s \Delta V_{C1}}$$ Equation 3.54

The minimum expected capacitances for $C_2$ and $C_3$ are given below.

$$C_2 \geq \frac{V_o d_2}{Rf_s(1-d_2)\Delta V_{C2}}$$ Equation 3.55

$$C_3 \geq \frac{V_o d_2}{Rf_s(1-d_2)\Delta V_{C3}}$$ Equation 3.56

The capacitor values obtained for $C_1$, $C_2$ and $C_3$ are 7.8 $\mu F$, 42.5 $\mu F$ and 31.8 $\mu F$ respectively.

### 3.8.3 Voltage Stress and NVS of Switches and Diodes

In order to properly design the converter, it is essential that the voltage stress of the semiconductor devices is taken into cognizance. The voltage stress of the device is also known as PIV. It is the maximum voltage encountered by the device without being destroyed when it is turned off. During CCM, the voltage stresses are given as

$$V_{S1} = V_{D1} = V_o - V_{C1}$$ Equation 3.57

$$V_{S2} = V_{Dm} = V_{C3}$$ Equation 3.58

$$V_{S3} = V_{S4} = V_{D3} = V_{D4} = V_{FD}$$ Equation 3.59

Where $V_{FD}$ is the forward voltage drop of the semiconductor device.

In the battery charging mode that is operation mode two, $V_{S3}$ and $V_{S4}$ are not equal. $V_{S3}$ remains the same as its $V_{FD}$ but $V_{S4}$ is determined by the battery voltage and the forward voltage drop of diodes, $D_{b1}$ and $D_{b2}$. Equation 3.40 then becomes

$$V_{S4} = V_b + V_{FD(D_{b1})} + V_{FD(D_{b2})} \quad \text{Equation 3.60}$$

$$V_{D2} = V_o - V_{C1} + V_{C3} \quad \text{Equation 3.61}$$

In the battery charging mode, $V_{S3}$ and $V_{S4}$ are equal. The voltage stress on $S_3$ and $S_4$ is determined by the battery voltage and the turn off period of the $V_{FD}$ of $D_{b1}$ and $D_{b2}$. Hence,

$$V_{S3} = V_{S4} = V_b + V_{FD(D_{b1turn-off})} + V_{FD(D_{b2turn-off})} \quad \text{Equation 3.62}$$

The normalised voltage stress (NVS) is the voltage stress of the semiconductor device divided by the total output voltage (Varesi et al., 2018a). The NVS of the switches/diodes are given as the

$$NVS_{S1} = NVS_{D1} = \frac{V_o - V_{C1}}{V_o} \quad \text{Equation 3.63}$$

$$NVS_{S2} = NVS_{Dm} = \frac{V_{C3}}{V_o} \quad \text{Equation 3.64}$$

$$NVS_{D2} = \frac{V_o - V_{C1} + V_{C3}}{V_o} \quad \text{Equation 3.65}$$

## 3.9 Dynamic Modeling of the Proposed BITIHGC

There are three power operation modes available for the suggested converter. Different control variables are needed to adjust the converter in each operating mode in order to control the output voltage and the power of the input sources. Two active-duty ratios ($d_1$, $d_2$) are used in the first power operation mode, while three alternative duty ratios ($d_1$, $d_2$, $d_4$) are selected for the second and third operating modes. It should be noted that $d_3$ plays no part in this modeling. This is because switch, $S_3$ functions to complete the circuit.

Designing closed-loop controllers for MIMO systems is challenging because of the multiple interaction control loops present in these systems (Qian et al., 2010). It is necessary to first obtain the small-signal model of the converter in order to develop closed-loop controllers for the proposed MIC. As can be seen from the topology description, the proposed BITIHGC consists of seven passive elements. These are $L_1$, $L_2$, $L_3$, $C_1$, $C_2$, $C_3$ and $C_o$. Six state variables are introduced. These are $L_1$, $L_2$, $C_1$, $C_2$, $C_3$ and $C_o$.

For the first operation mode, the state-space model can be represented using the volt-second balance theory for inductors and the ampere-second balance theory for capacitors;

$$L_1 \frac{di_{L1}}{dt} = d_1 v_1 + (1 - d_1)(v_1 + v_{co} - v_o) \quad \text{Equation 3.66}$$

$$L_2 \frac{di_{L2}}{dt} = d_2 v_2 + (1 - d_2)(v_2 - v_{c3}) \quad \text{Equation 3.67}$$

$$C_1 \frac{dv_{c1}}{dt} = (1 - d_2) i_{L1} + i_{L2} + (1 - d_1)(-2\frac{v_o}{R_L}) \quad \text{Equation 3.68}$$

$$C_2 \frac{dv_{c2}}{dt} = d_2(i_{L1} + i_{L2}) + (1 - d_2)(-i_{L1} + i_{L2}) \quad \text{Equation 3.69}$$

$$C_3 \frac{dv_{c3}}{dt} = (1 - d_2) i_{L2} + d_2(-2\frac{v_o}{R_L}) \quad \text{Equation 3.70}$$

$$C_o \frac{dv_o}{dt} = (1 - d_1)(2i_{L1} - \frac{v_o}{R_L}) + d_1(-\frac{v_o}{R_L}) \quad \text{Equation 3.71}$$

In a similar manner, the state-space model for operation mode two can be written using the volt-second balance theory for inductors and the ampere-second balance theory for capacitors;

$$L_1 \frac{di_{L1}}{dt} = d_1 v_1 + d_4 v_b + (1 - d_1)(d_4 v_b + v_1 + v_{co} - v_o) \quad \text{Equation 3.72}$$

$$L_2 \frac{di_{L2}}{dt} = d_2 v_2 + d_4 v_b + (1 - d_2)(d_4 v_b + v_2 - v_{c3}) \quad \text{Equation 3.73}$$

$$C_1 \frac{dv_{c1}}{dt} = (1 - d_2) i_{L1} + i_{L2} + (1 - d_1)(-2\frac{v_o}{R_L}) \quad \text{Equation 3.74}$$

$$C_2 \frac{dv_{c2}}{dt} = d_2(i_{L1} + i_{L2}) + (1 - d_2)(-i_{L1} + i_{L2}) \quad \text{Equation 3.75}$$

$$C_3 \frac{dv_{c3}}{dt} = (1 - d_2) i_{L2} + d_2(-2\frac{v_o}{R_L}) \quad \text{Equation 3.76}$$

$$C_o \frac{dv_o}{dt} = (1 - d_1)(2i_{L1} - \frac{v_o}{R_L}) + d_1(-\frac{v_o}{R_L}) \quad \text{Equation 3.77}$$

The state-space model for the third operation mode can be written using the volt-second balance theory for inductors and the ampere-second balance theory for capacitors;

$$L_1 \frac{di_{L1}}{dt} = d_1 v_1 - (d_1 - d_4) v_b + (1 - d_1)(v_1 + v_{co} - v_o) \quad \text{Equation 3.78}$$

$$L_2 \frac{di_{L2}}{dt} = d_2 v_2 + (d_2 - d_4)\, v_2 - v_{C3} - v_b \quad \text{Equation 3.79}$$

$$C_1 \frac{dv_{c1}}{dt} = (1 - d_2) i_{L1} + i_{L2} + (1 - d_1)(-2 \frac{v_o}{R_L})$$ Equation 3.80

$$C_2 \frac{dv_{c2}}{dt} = d_2 (i_{L1} + i_{L2}) + (1 - d_2)(-i_{L1} + i_{L2})$$ Equation 3.81

$$C_3 \frac{dv_{c3}}{dt} = (1 - d_2) i_{L2} + d_2 (-2 \frac{v_o}{R_L})$$ Equation 3.82

$$C_o \frac{dv_o}{dt} = (1 - d_1)(2 i_{L1} - \frac{v_o}{R_L}) + d_1 (- \frac{v_o}{R_L})$$ Equation 3.83

It is assumed that two components make up the state variables, duty ratios, and input voltages (Nejabatkhah et al., 2012). These are perturbations ($\tilde{x}$, $\tilde{d}$, $\tilde{v}$) and dc values ($\bar{X}$, $\bar{D}$, $\bar{V}$) expressed as;

$$x = \bar{X} + \tilde{x};\ d = \bar{D} + \tilde{d};\ v = \bar{V} + \tilde{v}$$ Equation 3.84

By ignoring the second-order elements and assuming that the perturbations are modest and do not change dramatically over the course of a single switching period, small-signal models are produced. The small-signal models in matrix form are as follows;

$$\dot{x} = A\tilde{x} + B\tilde{u}$$ Equation 3.85

$$y = C\tilde{x} + D\tilde{u}$$ Equation 3.86

In Equation 3.66, $\tilde{x}$ is the state variable vector, and $\tilde{u}$ is the control variables vector. In Equation 3.67, $\tilde{y}$ is the output vector.

For the first operation mode, the matrix form of the small-signal model is;

$$A=\begin{bmatrix} 0 & 0 & \frac{1-\bar{D}_1}{L_1} & 0 & 0 & \frac{\bar{D}_1-1}{L_1} \\ 0 & 0 & 0 & 0 & \frac{\bar{D}_2-1}{L_2} & 0 \\ \frac{1-\bar{D}_2}{C_1} & \frac{1-\bar{D}_2}{C_1} & 0 & 0 & 0 & \frac{2-2\bar{D}_1}{R_L C_1} \\ \frac{\bar{D}_2}{C_2} & \frac{2\bar{D}_2-2}{C_2} & 0 & 0 & 0 & 0 \\ -\frac{\bar{D}_2}{C_3} & \frac{1-\bar{D}_2}{C_3} & 0 & 0 & 0 & 0 \\ \frac{2-2\bar{D}_1}{C_o} & 0 & 0 & 0 & 0 & -\frac{1}{R_L C_o} \end{bmatrix}, B=\begin{bmatrix} \frac{\bar{V}_O-\bar{V}_{C1}}{L_1} & 0 \\ 0 & \frac{\bar{V}_{C3}}{L_2} \\ \frac{\bar{I}_{L1}}{2C_1} & \frac{\bar{I}_{L2}-\bar{I}_{L1}}{C_1} \\ 0 & \frac{2\bar{I}_{L2}}{C_2} \\ 0 & -\frac{\bar{I}_{L2}}{C_3} \\ -\frac{\bar{I}_{L1}}{C_o} & 0 \end{bmatrix}$$

Equation 3.87

$$C=\begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix},\ \tilde{x}=\begin{bmatrix} \tilde{\imath}_{L1} \\ \tilde{\imath}_{L2} \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{C3} \\ \tilde{v}_o \end{bmatrix}, \tilde{u}=\begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \end{bmatrix}, D=0$$

Equation 3.88

For the second operation mode, the matrix form of the small signal model is;

$$A = \begin{bmatrix} 0 & 0 & \frac{1-\bar{D}_1}{L_1} & 0 & 0 & \frac{\bar{D}_1-1}{L_1} \\ 0 & 0 & 0 & 0 & \frac{\bar{D}_2-1}{L_2} & 0 \\ \frac{1-\bar{D}_2}{C_1} & \frac{1-\bar{D}_2}{C_1} & 0 & 0 & 0 & \frac{2-2\bar{D}_1}{R_L C_1} \\ \frac{\bar{D}_2}{C_2} & \frac{2\bar{D}_2-2}{C_2} & 0 & 0 & 0 & 0 \\ -\frac{\bar{D}_2}{C_3} & \frac{1-\bar{D}_2}{C_3} & 0 & 0 & 0 & 0 \\ \frac{2-2\bar{D}_1}{C_o} & 0 & 0 & 0 & 0 & -\frac{1}{R_L C_o} \end{bmatrix}, \quad \text{Equation 3.89}$$

$$\mathrm{B} = \begin{bmatrix} \frac{\bar{V}_O-\bar{V}_{C1}}{L_1} & 0 & \frac{2\bar{V}_B}{L_1} \\ 0 & \frac{\bar{V}_{C3}}{L_2} & \frac{V_B}{L_2} \\ \frac{\bar{I}_{L1}}{2C_1} & \frac{\bar{I}_{L2}-\bar{I}_{L1}}{C_1} & 0 \\ 0 & \frac{2\bar{I}_{L2}}{C_2} & 0 \\ 0 & -\frac{\bar{I}_{L2}}{C_3} & 0 \\ -\frac{\bar{I}_{L1}}{C_o} & 0 & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \ \tilde{x} = \begin{bmatrix} \tilde{\imath}_{L1} \\ \tilde{\imath}_{L2} \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{C3} \\ \tilde{v}_o \end{bmatrix}, \tilde{u} = \begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \\ \tilde{d}_4 \end{bmatrix}, D = 0 \quad \text{Equation 3.90}$$

For the third operation mode, the matrix form of the small signal model is;

$$A = \begin{bmatrix} 0 & 0 & \frac{1-\bar{D}_1}{L_1} & 0 & 0 & \frac{\bar{D}_1-1}{L_1} \\ 0 & 0 & 0 & 0 & \frac{\bar{D}_2-1}{L_2} & 0 \\ \frac{1-\bar{D}_2}{C_1} & \frac{1-\bar{D}_2}{C_1} & 0 & 0 & 0 & \frac{2-2\bar{D}_1}{R_L C_1} \\ \frac{\bar{D}_2}{C_2} & \frac{2\bar{D}_2-2}{C_2} & 0 & 0 & 0 & 0 \\ -\frac{\bar{D}_2}{C_3} & \frac{1-\bar{D}_2}{C_3} & 0 & 0 & 0 & 0 \\ \frac{2-2\bar{D}_1}{C_o} & 0 & 0 & 0 & 0 & -\frac{1}{R_L C_o} \end{bmatrix}, \quad \text{Equation 3.91}$$

$$\mathrm{B} = \begin{bmatrix} \frac{\bar{V}_O-\bar{V}_{C1}-\bar{V}_B}{L_1} & 0 & \frac{\bar{V}_1-\bar{V}_B}{L_1} \\ 0 & \frac{\bar{V}_2}{L_2} & \frac{\bar{V}_2-\bar{V}_{C3}-\bar{V}_B}{L_2} \\ \frac{\bar{I}_{L1}}{2C_1} & \frac{\bar{I}_{L2}-\bar{I}_{L1}}{C_1} & 0 \\ 0 & \frac{2\bar{I}_{L2}}{C_2} & 0 \\ 0 & -\frac{\bar{I}_{L2}}{C_3} & 0 \\ -\frac{\bar{I}_{L1}}{C_o} & 0 & 0 \end{bmatrix}$$

$$C = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}, \ \tilde{x} = \begin{bmatrix} \tilde{\imath}_{L1} \\ \tilde{\imath}_{L2} \\ \tilde{v}_{C1} \\ \tilde{v}_{C2} \\ \tilde{v}_{C3} \\ \tilde{v}_o \end{bmatrix}, \tilde{u} = \begin{bmatrix} \tilde{d}_1 \\ \tilde{d}_2 \\ \tilde{d}_4 \end{bmatrix}, D = 0 \quad \text{Equation 3.92}$$

## 3.10 Proposed Energy Management of BITIHGC

For hybrid MICs, it is essential that an algorithm is developed to determine the appropriate operation mode. The PV port is the first input port while the FC port is the second input port. The operation scenarios may occur when there is poor output power from the PV

or higher load requirements. The proposed BITIHGC should be able to serve the load provided any one of the input sources and battery storage contains sufficient power.

It is important to identify minimum power levels required for proper operation of the converter modes. The power from the FC ($P_{FC}$) should be taken into consideration same as the minimum power from the PV ($P_{PV}$). The battery should have upper and lower *SOC* references ($B_L$ and $B_U$). Also, the load power requirement, $P_L$ must be taken into cognisance. The algorithm for the energy management of the proposed BITIHGC is presented in Figure 3.18. The power management procedure is described.

i. In event of lower load, $P_L$ should be compared to either of $P_{PV}$ and $P_{FC}$ or their sum, $P_{PV} + P_{FC}$. In the proposed algorithm, $P_{PV}$ is considered first. If $P_{PV}$ can satisfy the load, $P_L$, then the *SOC* is checked to verify if it is greater than $B_U$. When the *SOC* is greater than $B_U$, the first operation mode is adopted. This is the battery bypassing mode.

ii. When $P_{PV}$, $P_{FC}$, or $P_{PV} + P_{FC}$ cannot serve the load, the algorithm will check if *SOC* is greater than $B_U$. If $SOC > B_U$, the second operation mode is adopted. This is the battery discharging mode. It further checks if $SOC < B_L$. So long as $B_L > SOC$, the battery discharging mode continues. If $SOC < B_L$, the algorithm returns to the start position or command.

iii. As can be seen from the algorithm, the third operation mode is adopted when $P_{PV}$, $P_{FC}$ or $P_{PV} + P_{FC}$ is greater than $P_L$ and $SOC < B_L$.

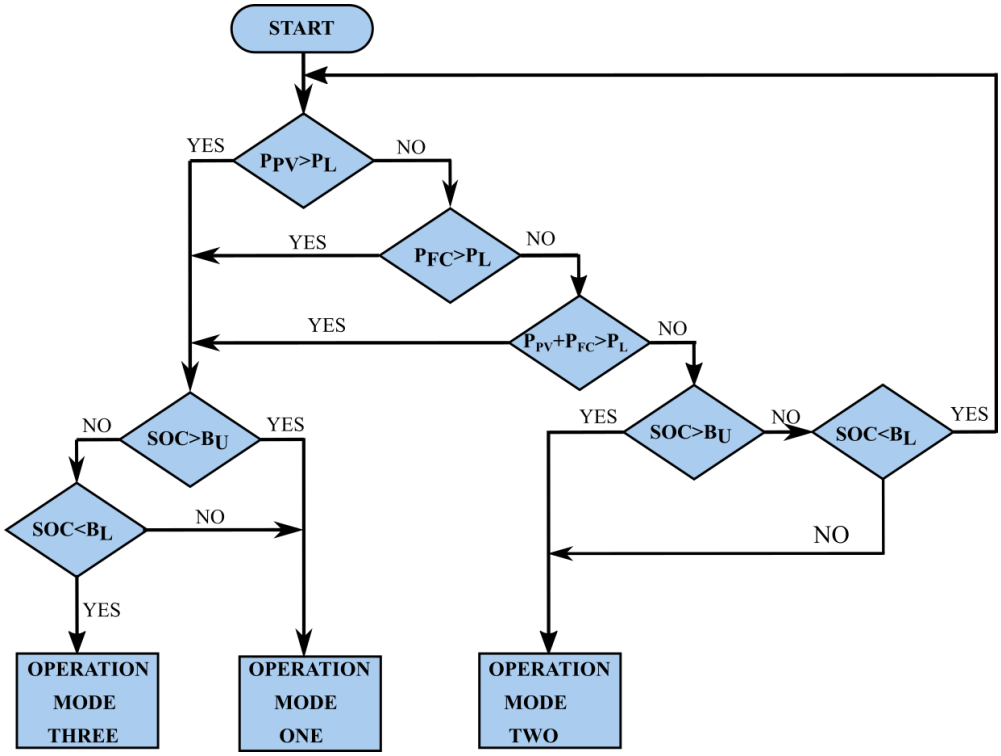


**Figure 3.18:** Algorithm for Energy Management of the Proposed BITIHGC

## 3.11 Proposed Control of Converter

In this proposed BITIHGC, the two separate RE sources are combined with a battery input to satisfy varying load requirements. The BITIHGC is designed to draw a different amount of power from the amalgamation of RE sources while appropriating the power demand of the load at regulated output voltage. The ANN strategy was used in this project. The strategy adopted is based on previous work done in Utomo et al. (2011).

### 3.11.1 Block Diagram of Proposed Control

The commuting switches are operated via a PWM technology. The converter's output voltage is controlled and managed by the ANN control algorithm that is used. Figure 3.19 presents a schematic of the voltage controller. All four duty ratios were controlled. However, the duty ratios, $d_3$ and $d_4$ can be constant depending on the operation mode. For example,

their function during the first operation mode where they provide the current path that completed the circuit.

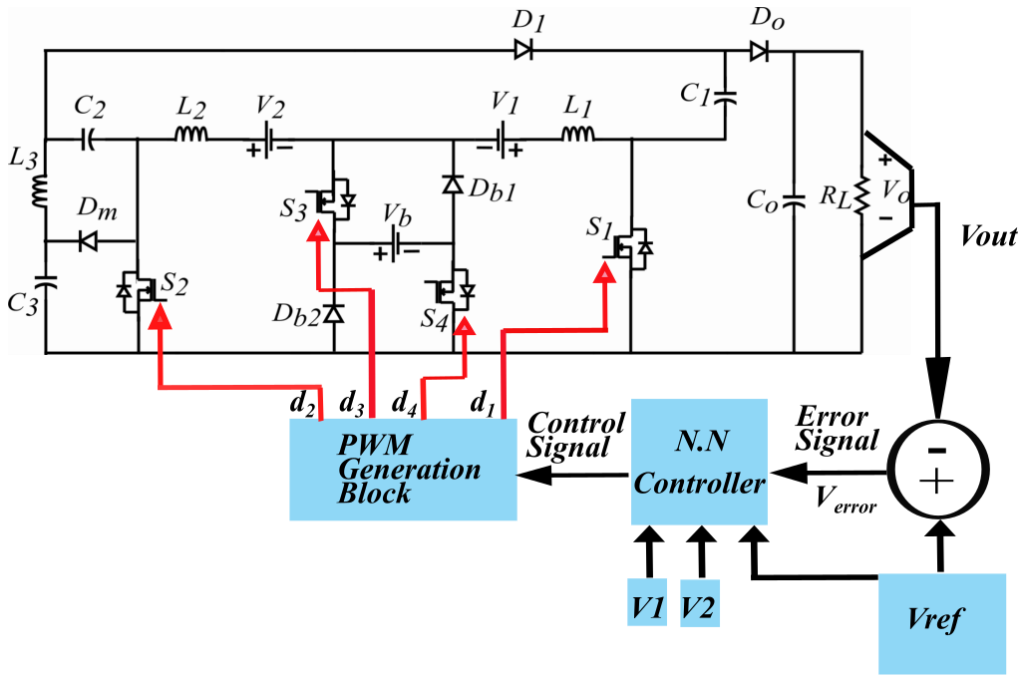


**Figure 3.19:** Voltage Controller Design

There are four voltages: $V_1$, $V_2$, *Vref*, the reference voltage, and *Vout*, the measured output voltage. The error signal generated after the summing point, is fed into neural network (NN) controller. The NN controller produces the actuating signal. A comparison is done between the control signal a repeating sequence signal or carrier wave. The switching signal that is generated, contains the necessary duty cycles for maintenance of the reference voltage value.

### 3.11.2 Architecture of Neural Network Control

In designing the NN control, the entire plant is considered. Each layer's input and output neuron count should match the system's input and output signal count. The

architecture of the adapted NN control for the three-input high gain boost converter is as shown in Figure 3.19. There are four inputs to the input layer. These are $V_1$, $V_2$, $V_{error}$ and $V_{ref}$. There are four outputs, $d_1$, $d_2$, $d_3$ and $d_4$.

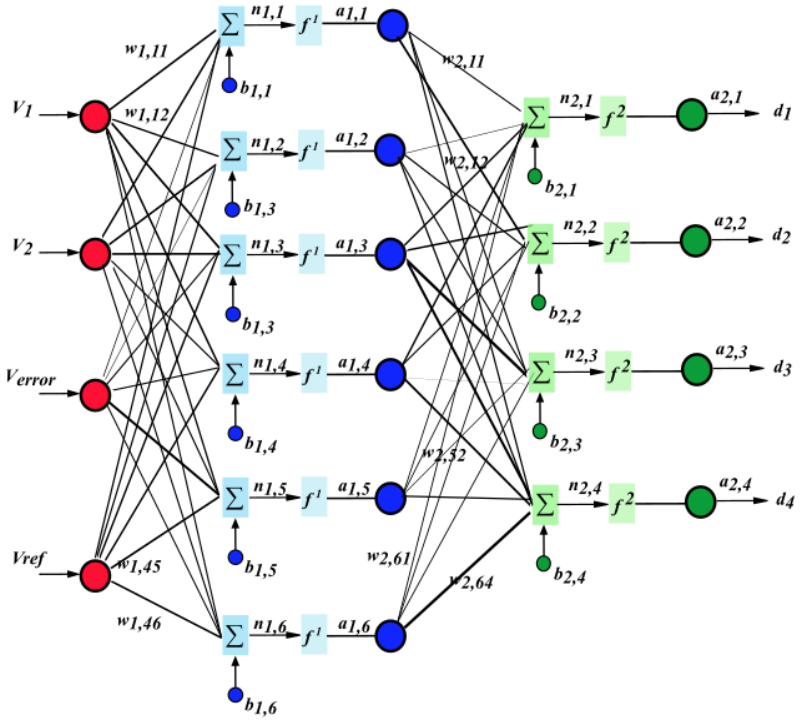


**Figure 3.20:** Architecture of the Adapted Neural Network Controller

This formation is dependent on the number of neurons in each layer of the proposed NN controller architecture. The input neurons are contained in the input layer. The error signal, which is difference between the desired output voltage signal and actual output voltage signal, is directed to the first input neuron. The hidden layer has six neurons. The output layer has two neurons.

There are some important parameters that must be computed in the process of formulating the NN control. From Figure 3.20, the connection existing between the hidden layer and the input layer is supported by weight factors which are represented by $w_{1,11}$, $w_{1,12}$,

etc. The bias is represented by $b_{1,11}$, $b_{1,12}$, etc. The total input net of the hidden layer can be computed by;

$$net_{ij} = \sum_{i=1}^{4} w_{ij} x_i \qquad \text{Equation 3.93}$$

Where *x* represents the input data, *j* represents the parameters of the weights, and *i* = 1,2,3.

The output function of a neuron is represented by *a*. This output function is dependent on the activation function of the layer, *f* and the transfer function of the network, $n_i$ at that particular layer. Hence, the output of the neuron can be computed by;

$$a_i = f(n_i) \qquad \text{Equation 3.94}$$

The transfer function of the network can be computed as;

$$n_i = \sum_{j=1}^{s} w_{ij} a_j + b_i \qquad \text{Equation 3.95}$$

This work has adopted the tangent hyperbolic activation function for the hidden layer. The activation function influences the state of the neurons in the layer. The choice of the tanh activation function over the sigmoid activation function, is based on its faster learning capacity and strong gradients. The activation function can be computed by;

$$f(n_i) = \frac{2}{1 + e^{-2n_i}} - 1 \qquad \text{Equation 3.96}$$

Some parameters that impact on the update of the bias and connection weights are the sampling time, *k*, the learning rate, α and the performance index function of the network, *F*. Hence, the equations to update the respective weights and bias are;

$$w_{ij}(k+1) = w_{ij} - \alpha \frac{\partial F(k)}{\partial w_{ij}}$$ Equation 3.97

$$b_{ij}(k+1) = b_{ij} - \alpha \frac{\partial F(k)}{\partial b_{ij}}$$ Equation 3.98

3.11.2.1 Backpropagation Learning Algorithm for Training

Following the modelling of the NN architecture, the next step is defining the learning model that is required in order to update the network parameters. Generally, for NN controller in the learning mode, ample data is a requirement for training that provides input-output mapping data of the plant. The online learning Backpropagation is adopted and the algorithm is developed.

The performance index function, *F* is given by;

$$F(k) = \frac{1}{2} \sum_{i} e_i^2\,(k)$$ Equation 3.99

where $e_i$ is the sum of square error, and is computed by;

$$e_i(k) = t_i(k) - a_i(k)$$ Equation 3.100

In Equation 3.54, $t_i$ represents the target signal while $a_i$ represents the output signal on the last layer.

The good fitting accuracy of the gradient descent method of training makes it the adopted training method of the back propagation learning algorithm. Hence, for the performance index, the gradient descent with respect to the weights is defined by;

$$\frac{\partial F}{\partial w_{ij}} = \frac{\partial F \partial n_i}{\partial n_i \partial w_{ij}}\, f(n_i)$$ Equation 3.101

The sensitivity can be computed by;

$$S_i = \frac{\partial F}{\partial n_i}$$ Equation 3.102

$$S_i^m = \frac{\partial F a_i}{\partial a_i \partial n_i}$$ Equation 3.103

For the network transfer function, the gradient descent with respect to the weight is defined by;

$$\frac{\partial n_i}{\partial w_{ij}} = a_i$$ Equation 3.104

If Equation 3.84 and Equation 3.85 are substituted into Equation 3.37, the updating connection parameter can be obtained as;

$$w_i(k+1) = w_i(k) - \alpha s_i(k) a_i(k)$$ Equation 3.105

Applying the same technique, the updating bias parameter can be obtained as;

$$b_i(k+1) = b_i(k) - \alpha s_i(k)$$ Equation 3.106

## 3.12 Offline Training of Neural Network

The three stages of neural network training are training, verification, and testing. The training was guided by predetermined targets and inputs. The samples were separated into training, verification, and testing samples and arranged in a random order. The data was obtained via simulation. 100,000 samples were used for the entire training process. Out of these 100,000 samples, 70,000 samples were used for training, 15,000 samples were applied during validation while 15,000 samples were applied for testing. The weights and bias were updated in order to train the network.

The formation of the trained network is shown in Figure 3.21. It highlights the six neurons in the hidden layer. The regression plot after training in Figure 3.22 shows the closeness to unity which indicated good performance of the training, validation and testing. The effectiveness of the offline trained NN was only applicable to the software simulation. During real hardware implementation, the non-ideal components come into play, thus causing lower values in the voltage output. This necessitated the online training which used the back propagation learning algorithm presented in subchapter 3.11.2.1.

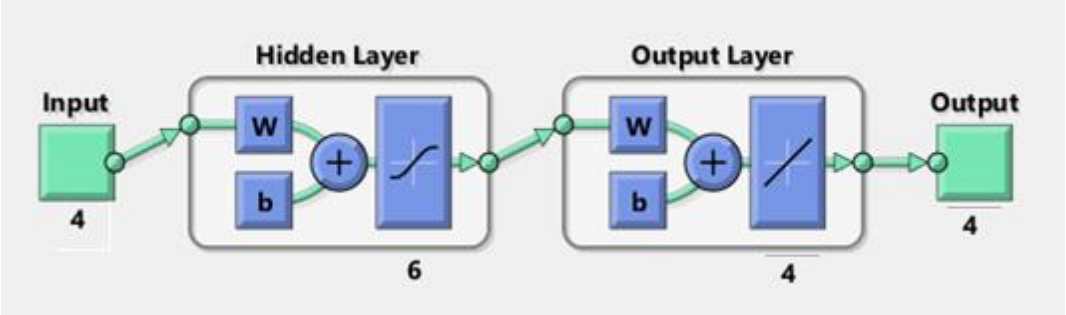


**Figure 3.21:** Formation of Trained Neural Network

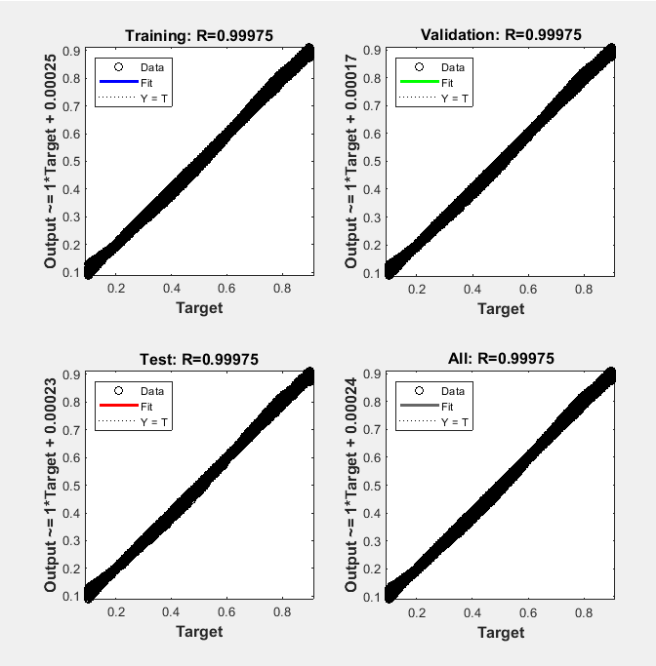


**Figure 3.22:** Regression Plot Obtained after Training of Data

## 3.13 Open Loop Simulation Model of the Proposed Converter

The simulation model of the proposed converter was developed using MATLAB/ Simulink. Since there are three operation modes, two models must be developed. One for the first operation mode, and the second for operation modes two and three. These simulation models are restricted to open loop models and are presented in the following sub-sections.

### 3.13.1 Open Loop Simulation Model for Operation Mode One

In operation mode one, there are two inputs in the simulation model. The simulation model is shown in Figure 3.23. The model contains the converter circuit block and the PWM generator block. The converter circuit block consists of electronic power switches, inductors, capacitors and diodes. The IGBT is adopted for power switches. In this mode, the DC input voltages are set as $V_1$ = 12 $V$, and $V_2$ = 24 $V$.

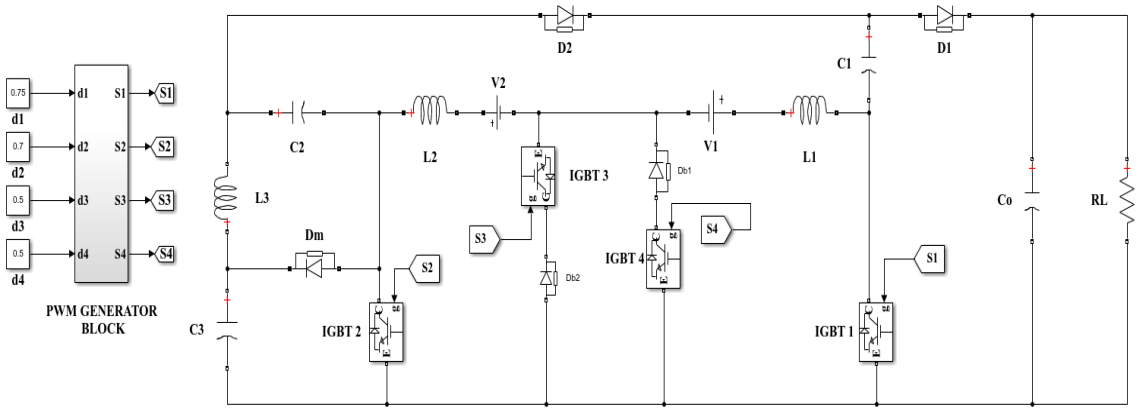


**Figure 3.23:** Open Loop Simulation Model for Operation Mode One

The PWM generator block provides the switching signals that are sent to the respective switches. To generate the switching signals, the duty ratios and switching frequency are compared as done in PWM. The PWM, determines the width of the switching pattern. S-function blocks are developed and assigned for each switching signal. The S-function blocks for the respective signals are shown in Figure 3.24. The desired frequency of 15 *kHz* is embedded in the code as can be seen in **Appendix D**.

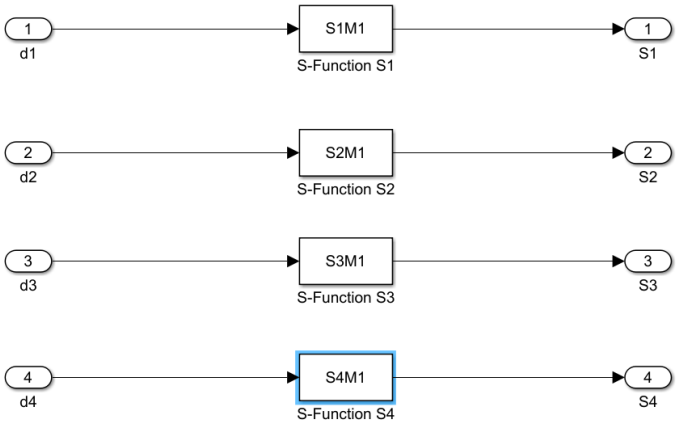


**Figure 3.24:** S-function blocks for the Respective Switching Signals

### 3.13.2 Simulation Model for Operation Mode Two and Operation Mode Three

The simulation model for operation mode two and mode three is presented in Figure 3.25. The battery block has been inserted between the parallel switch/diode pairs. This inclusion of the battery block is the major similarity between the simulation models of operation mode two and operation mode three. The difference between operation modes two and three is the switching pattern and duty ratio of switches $S_3$ and $S_4$. The code for programming switches $S_3$ and $S_4$ in the operation modes are provided in **Appendix E**.

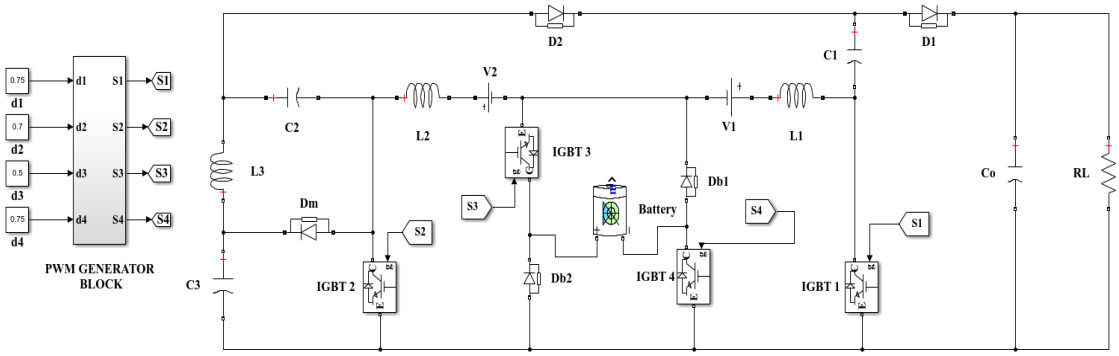


**Figure 3.25:** Open Loop Simulation model for Operation Modes Two and Three

## 3.14 Closed Loop Simulation Model

The closed loop simulation model is presented in Figure 4.17. In this schematic, all the components of the converter power boosting block, control and switching blocks have been interfaced. Compared with the open loop simulation model (Figure 3.23), the ANN controller loop has been added to the closed loop model. The error signal obtained from comparison of the output voltage and the reference voltage, *Vref*, feeds the ANN controller.

When the battery is bypassed, the control signal generated from the controller, is sent to switches, $S_1$ and $S_2$ only. Switches $S_3$ and $S_4$ are assigned permanent duty ratios. In the scenario where the battery is charged or discharged, switches, $S_1$, $S_2$ and $S_4$ will have to be controlled while $S_3$ is assigned a permanent duty ratio. The schematic of the simulation model for the ANN controller is presented in Figure 3.27. The relevant programming code has been developed using C++ and can be accessed in the **Appendix D**.

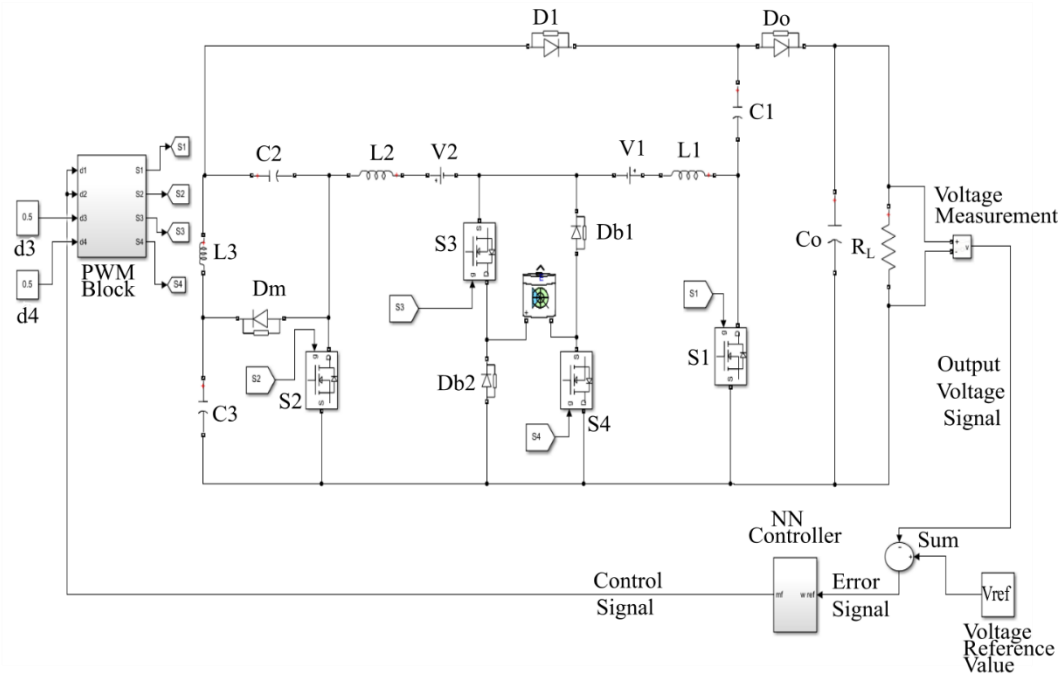


**Figure 3.26:** Closed Loop Simulation Model using Simulink Software

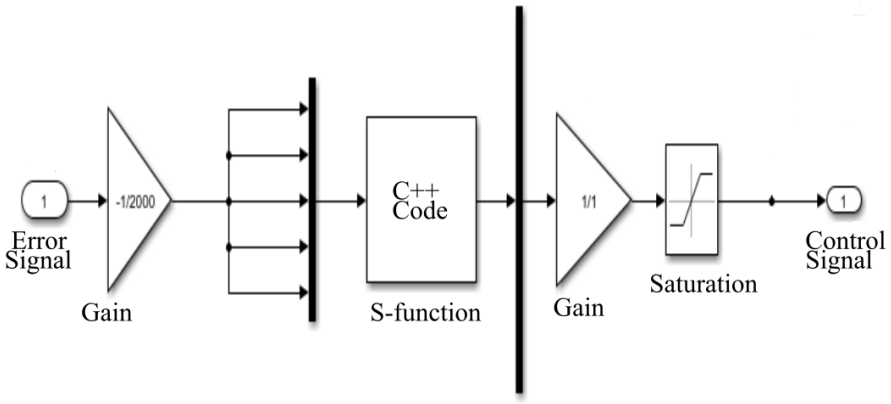


**Figure 3.27:** Simulation Model of Neural Network Controller using MATLAB Simulink Software

## 3.15 Hardware Development, Experimental Setup and Software Integration

There are two stages involved in the hardware development of the proposed converter. In the first stage, the PWM switching signals have to be generated. This stage is

known as software implementation. The PWM generator used in this project is the dSPACE 1104 controller board. The C code is embedded as a MATLAB script that is accessible to the real time interface (RTI) provided by the dSPACE Simulink environment. Figure 3.28 shows Simulink models that were built in the dSPACE environment for the respective open loop switching signals. The duty ratio is assigned a constant block as the control input. The duty ratio block is directed to the S-function block obtained from the simulation model. The digital I/O port of the controller accepts only Boolean format, hence the insertion of a Boolean converter. The gain block is positioned between the S-function and the Boolean converter. Each signal is sent to the digital I/O channel chosen. As can be observed from the Figure 3.28, the signals for $S_1$, $S_2$, $S_3$ and $S_4$ are assigned to channels 0, 4, 15 and 5 respectively. The digital I/O pin configuration of the dSPACE 1104 microcontroller board can be found in the appendices.

The dSPACE environment-based model for the closed loop control is depicted in Figure 3.29. The major difference is that an analogue to digital converter (ADC) block has been included. This ADC block, receives a feedback signal that represents the physical output voltage from the sensing element. The ADC converts this analogue feedback signal to a digital format and forwards to the comparator and controller for further processing. The use of gain blocks in the model is aimed at increasing or reducing the signals and logic to readable levels as required by the dSPACE controller board.

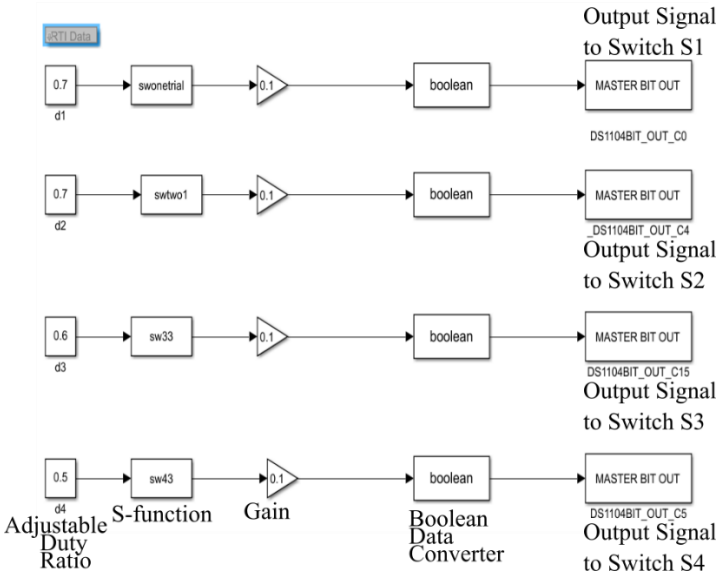


**Figure 3.28:** Simulink models in dSPACE environment for the experimental open loop switching signals

The second stage of the hardware development is the implementation of the converter circuit. Two variable DC supplies will represent the RE sources alongside a rechargeable battery. The power switches, diodes, inductors, and capacitors have to be assembled in accordance with the circuit design. Also included in this part is the decision for the feedback sensor and gate driver circuit.

The printed circuit board (PCB) of the prototype was designed using Proteus software and manufactured in the PCB lab. Thereafter, the electronic components selected were assembled and soldered on. The power switches chosen are high speed Infineon G25H1203 IGBTs. The output capacitor is a 270 $\mu F$ Nippon Chemicon electrolytic capacitor. Other capacitors are 100 $\mu F$ Elite capacitors. The selected inductor ratings are 350 $mH$ for $L_1$ and 200 $mH$ for the non-coupled inductors $L_2$ and $L_3$. The diodes are 20 $A$ axial silicon rectifier diodes. The datasheets of the components can be found in **Appendix H**.

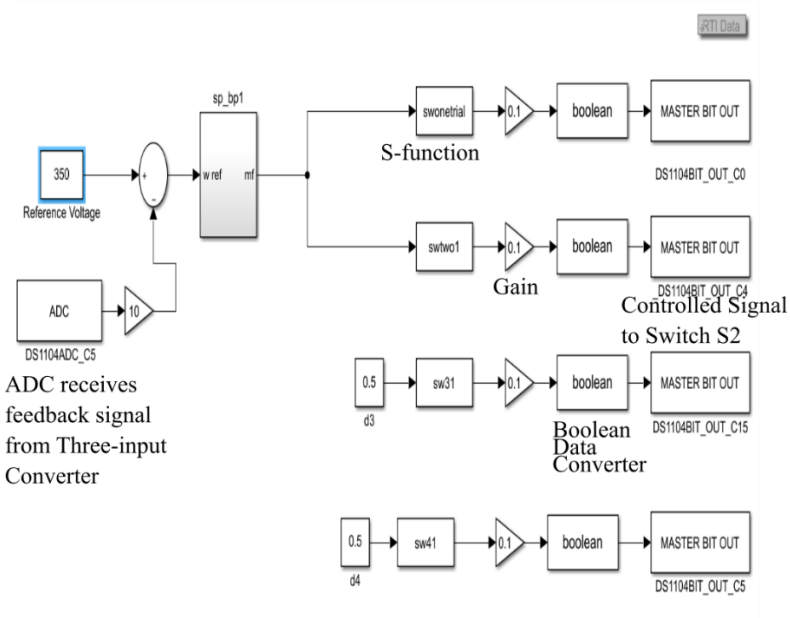


**Figure 3.29:** Simulink Closed Loop Experimental Control Model in dSPACE Environment

The nature of the hardware and software interfaces, imply that the software part be configured to control the hardware part. Figure 3.30 shows the process of integration for both hardware and software sides. The Simulink S-function which contains the C++ code is merged with the dSPACE model. This model is built and sent to the dSPACE ControlDesk software interface. The ControlDesk interface makes for easy manipulation of input values. In this case, we require to control the duty ratios of the switches. The signals from the ControlDesk platform are then sent to the selected digital output pins of the controller board. These output channels are chosen while developing the dSPACE model. The signals from the microcontroller are then directed to the gate driver. The gate driver provides isolation to the prototype and boosts the voltage level of the signal. Finally, the signal from the gate driver is forwarded to the power switches of the target prototype.

After all hardware and software components have been assembled, the system was set up for the conduction of experiments. Figure 3.31 shows the experimental setup. RE sources, $V_1$, and $V_2$, were replicated by laboratory DC power supplies, while a 12 $V$

rechargeable lead acid battery sufficed as the energy storage device. There is a dedicated gate driver for each power switch. This made it easy to troubleshoot in case of failure.

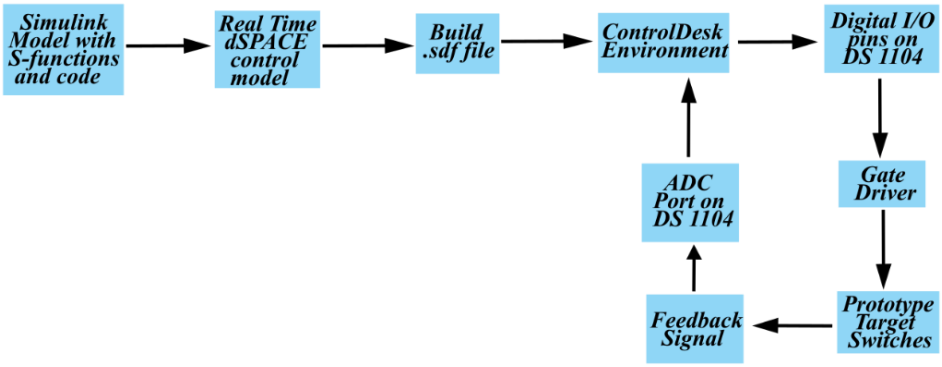


**Figure 3.30:** Hardware and Software Integration Process

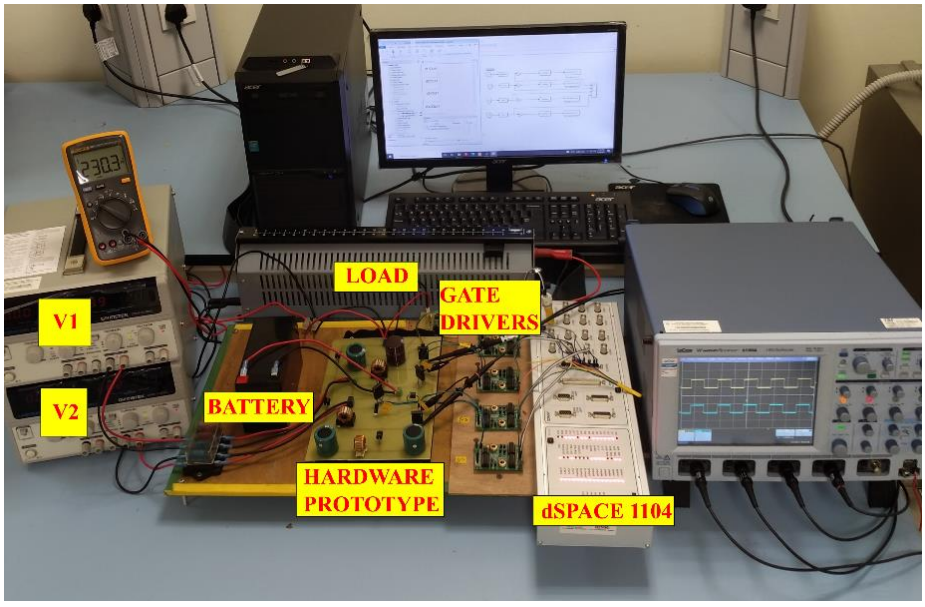


**Figure 3.31:** Laboratory set up for Experiments

## 3.16 Chapter Summary

The topology of the three-input high gain converter has been proposed and explained in this chapter. The combination of the boost and non-coupled inductor-based converter parts

have been depicted. Three operation modes and their respective switching states were outlined alongside the relevant equations. Each input port can deliver power to the load regardless of the status of the other input port. The output voltage and gain were derived for the different operation modes. Components selection and design identified the minimum values for the desired working condition. The dynamic modelling of the proposed BITIHGC has been presented.

The chapter also proposed a power management algorithm that would maximize power delivery to the load by switching between operation modes based on existing conditions. The ANN controller has been designed and the necessary parameters and equations have been defined. The offline and online training has been presented along with the simulation models, and hardware development.

# CHAPTER 4

# RESULTS AND DISCUSSION

## 4.1 Overview

Chapter 4 describes the processes involved in the software and hardware development of the proposed converter. It is essential that simulation of the proposed converter is carried out to verify the feasibility before validation via experiments. Thus, simulation results, prototype development process, and experimental results will be presented and discussed in this chapter.

## 4.2 Open Loop Simulation Results

The simulation of the proposed BITIHGC has been done to ascertain the converter response to the diverse situations. In the first scenario, unmatched voltage sources are applied to the converter. The battery port is disabled hence there is neither battery charging nor discharging. Since this is the primary operation mode, the converter's capacity to regulate the output voltage will be observed during this operation mode. The second scenario involves the battery discharging mode. In this case, lower voltage sources are applied to the converter. The battery discharge will be observed while simulating this scenario. In the third scenario, the same voltage levels as operation mode one, are applied in addition to battery charging functionality. The general simulation parameters are listed in Table 4.1.

**Table 4.1:** General Simulation Parameters

| Parameter | Value | Mode 1 | Mode 2 | Mode 3 |
|---|---|---|---|---|
| Switching Frequency | 15 kHz | - | - | - |
| Inductors, $L_1$, $L_2$, $L_3$ | 350, 200, 200 $mH$ | - | - | - |
| Capacitors, $C_o$, $C_1$, $C_2$, $C_3$ | 270, 100, 100, 100µ$F$ | - | - | - |

| | | | | |
|---|---|---|---|---|
| Load, $R_L$ (Ω) | 1000 | - | - | - |
| $V_1$ (V) | - | 12 | 6 | 12 |
| $V_2$ (V) | - | 24 | 12 | 24 |
| $V_b$, (V) | - | - | 12 | 12 |
| SOC (%) | - | - | 100 | 80 |
| $d_1$ (%) | - | 75 | 75 | 75 |
| $d_2$ (%) | - | 70 | 70 | 70 |
| $d_3$ (%) | - | 50 | 50 | 50 |
| $d_4$ (%) | - | 50 | 75 | 75 |

### 4.2.1 Open Loop Simulation Results for Operation Mode One

As listed in Table 4.1, the voltage sources in this operation mode are $V_1 = 12\ V$, and $V_2 = 24\ V$. The gate signals to $S_1$, $S_2$, $S_3$ and $S_4$ are shown in Figure 4.4. The alternate switching of $S_3$ and $S_4$ can be observed in the Figure. The width of $S_1$ and $S_2$ is due to the duty ratios of 0.75 and 0.7 respectively. The switching pulses are applied at the start-up to $S_1$, $S_2$ and $S_3$. The switching pulse to $S_4$ is applied only after $S_3$ conduction has ended and vice versa. Thus, $S_3$ and $S_4$ must never conduct at the same time. The turn-off period for $S_1$ is time, $t_1$ - $t_2$ while $S_2$ turns of during $t_2$ - $t_3$. The battery *SOC* profile has been excluded since the battery is bypassed during this mode.

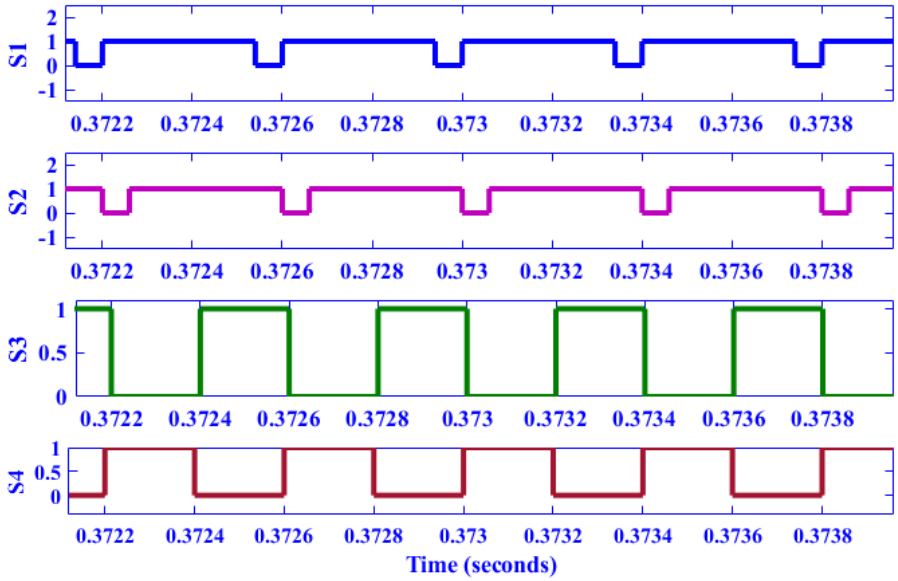


**Figure 4.1:** Simulated Gate Signals of the Switches for Operation Mode One

The input and output voltage levels are shown in Figure 4.5. The simulated output voltage is about 326.1 V while the output current is about 0.3261 A. The waveforms of the inductor currents, $i_{L1}$, $i_{L2}$ and $i_{L3}$ are displayed in Figure 4.6. The CCM operation of the proposed converter is thus confirmed. The respective ripple currents are less than ten percent. The inductor $L_1$ discharges during $t_1$ - $t_2$ and is charged by $V_1$ for the rest of the time period, during which the current rises. In same fashion, inductors $L_2$ and $L_3$ discharge during $t_2$-$t_3$ and is charged by $V_2$ and $V_{C3}$ respectively for the rest of the time period. The current flowing through inductor $L_3$ is a replica of the output current, $i_{out}$.

The waveforms of the inductor voltages are shown in Figure 4.7. At the beginning, the inductor $L_1$ is energized by 12 $V$ from $V_1$. In the second switching state, the inductor first discharges to $V_1 + V_{C1} - V_o$ (about -54 $V$) and further to -78 $V$ due to $V_2$ ($V_1 + V_{C1} - V_o - V_2$). Inductor $L_2$ is energized for the first two switching states by $V_2$. It initially discharges with a

voltage around -104 $V$ ($V_2 - V_{C2}$) during the third switching state and further by -138 $V$ due to $V_1$ ($V_2$ -$V_{C2} - V_{C1}$ - $V_1$).

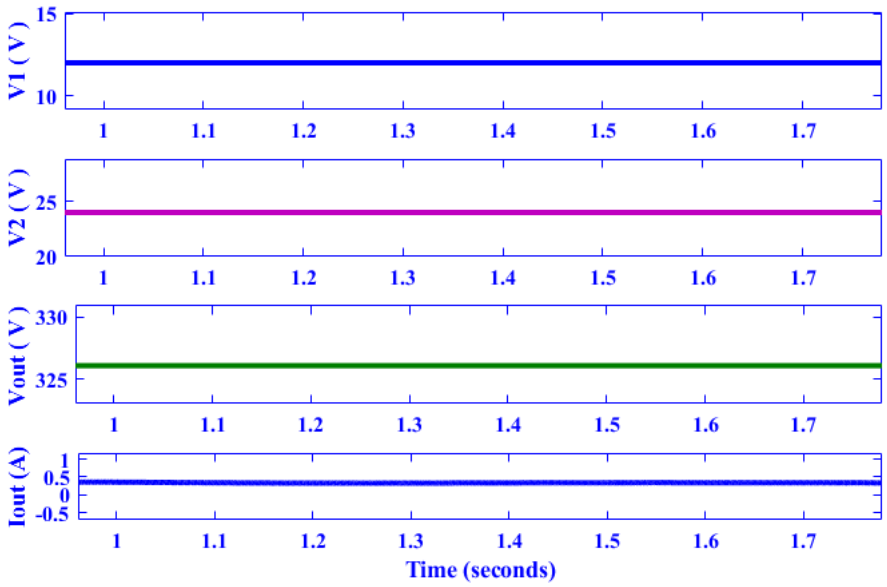


**Figure 4.2:** Simulated Voltage and Current Levels for Operation Mode One ( $V_1$, $V_2$ , $V_{out}$ *and* $I_{out}$)

In Figure 4.8, the voltage waveforms of capacitors, $C_1$, $C_2$ and $C_3$ are presented. It can be observed that capacitor $C_1$ discharges during $t_1$ - $t_2$, charges during $t_2$ - $t_3$, and is idle during t = $t_0$ - $t_1$ and $t_3$ - $t_4$. Capacitor, $C_2$ is discharged during $t_2$ - $t_3$ but charges during other states while $C_3$ charges during $t_2$ - $t_3$ but discharges during other states. The simulated waveforms of voltage stress on the power switches are shown in Figure 4.9. These results of the switch voltage stress will be further discussed during the presentation of the experimental results.

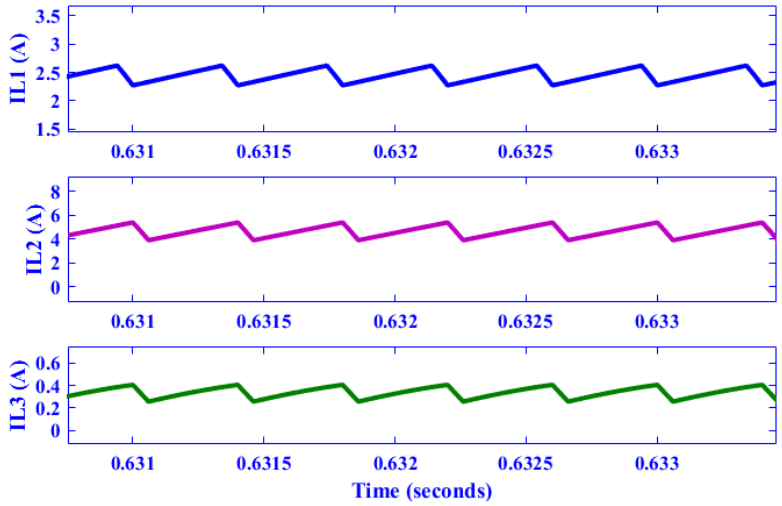


**Figure 4.3:** Inductors Current Waveforms for OperationMode One( $i_{L1}$, $i_{L2}$ and $i_{L3}$)

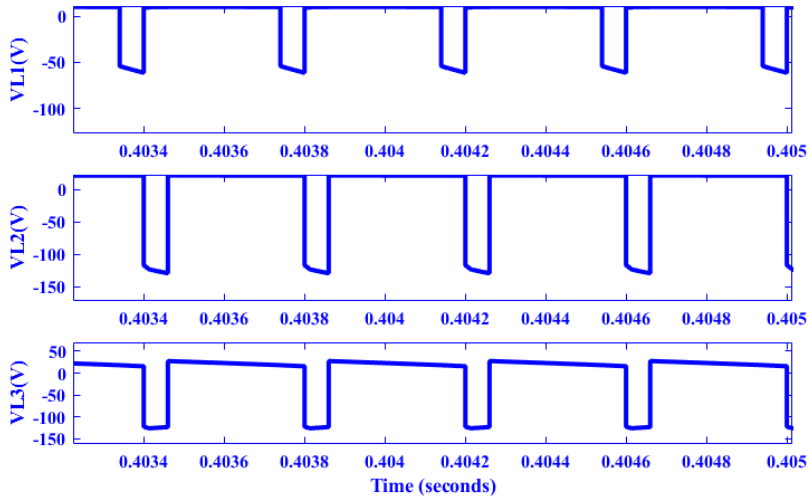


**Figure 4.4:** Simulated Inductor Voltage Waveforms ( $V_{L1}$, $V_{L2}$ *and* $V_{L3}$)

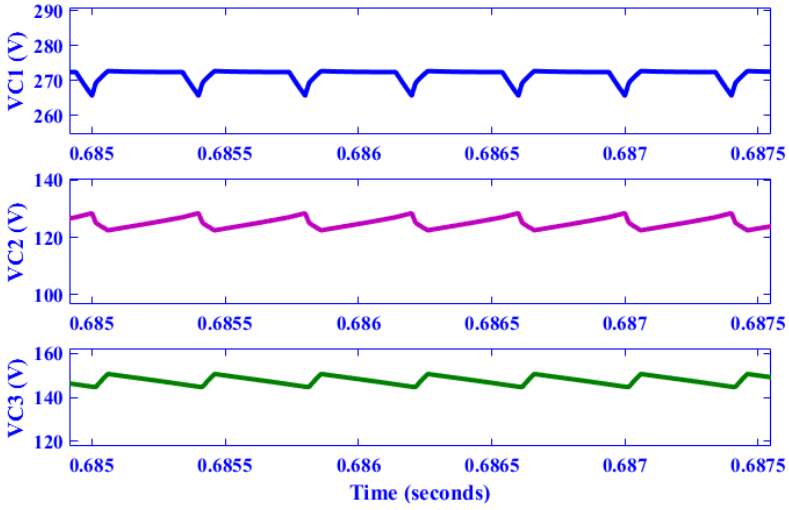


**Figure 4.5:** Simulated Capacitor Voltage Waveforms for Operation Mode One ($V_{C1}$, $V_{C2}$ and $V_{C3}$)

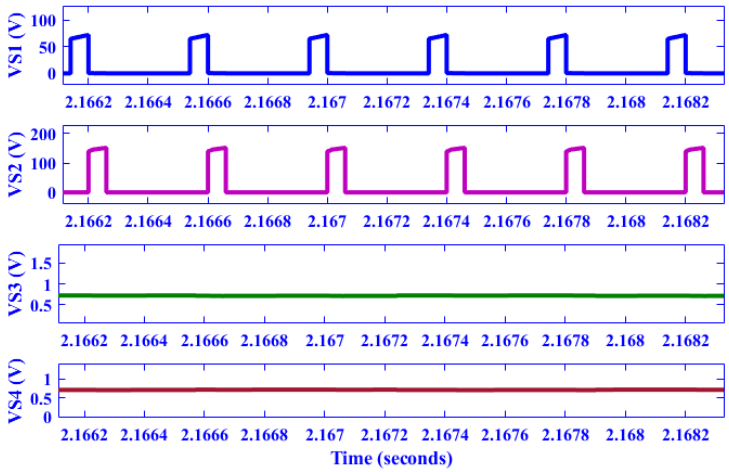


**Figure 4.6:** Switch Voltage Waveforms for Operation Mode One ($V_{S1}$, $V_{S2}$, $V_{S3}$ and $V_{S4}$)

### 4.2.2 Open Loop Simulation Results for Operation Mode Two

The gate signals for this operation mode are depicted in Figure 4.10. It can be noticed that the switching patterns for $S_1$ and $S_2$ remain unchanged from that of the first operation mode. The major difference is that of $S_4$ that is similar to $S_1$. The input voltages are $V_1$ = 6 $V$, $V_2$ = 12 $V$ and $V_b$ = 12 $V$. The output voltage and battery $SOC$ is shown in Figure 4.11.

The downward slope of the battery *SOC* indicates the depletion of the battery during operation. The simulated output voltage is about 318.5 *V*.

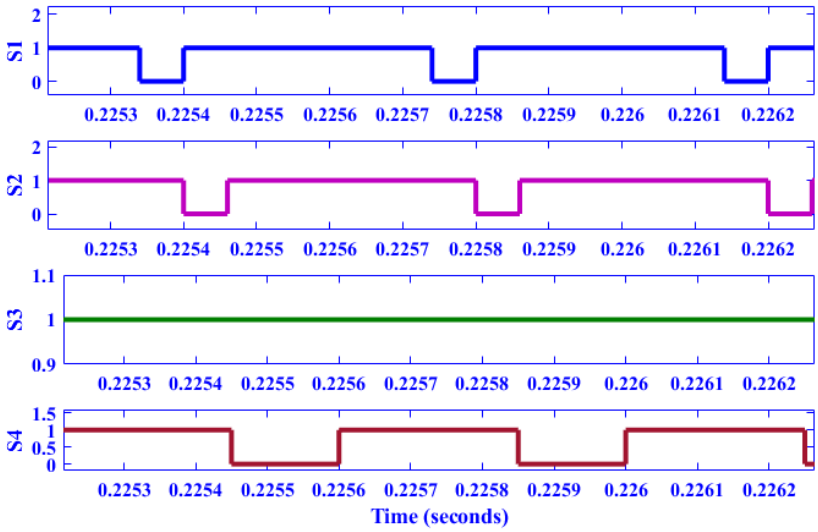


**Figure 4.7:** Simulated Gate Signals of the Switches for Operation Mode Two

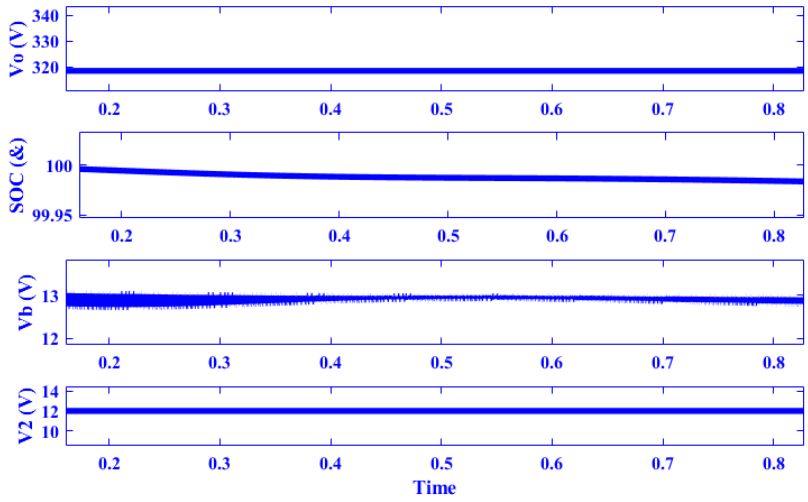


**Figure 4.8:** Voltage Levels and SOC Profile for Operation Mode Two

### 4.2.3 Open Loop Simulation Results for Operation Mode Three

The gate signals for this operation mode are depicted in Figure 4.12. It can be noticed that the switching patterns for $S_1$ and $S_2$ remain unchanged from that of the first and second operation modes. The major difference is that of $S_3$ is permanently at logic 0. The duty ratio of $S_4$ determines the charging rate of the battery. The unmatched voltages are $V_1 = 12\ V$ and $V_2 = 24\ V$. The output voltage and battery *SOC* is shown in Figure 4.13. The simulated output voltage is about 302.1 *V*. The upward slope of the battery *SOC* indicates the charging of the battery during operation.

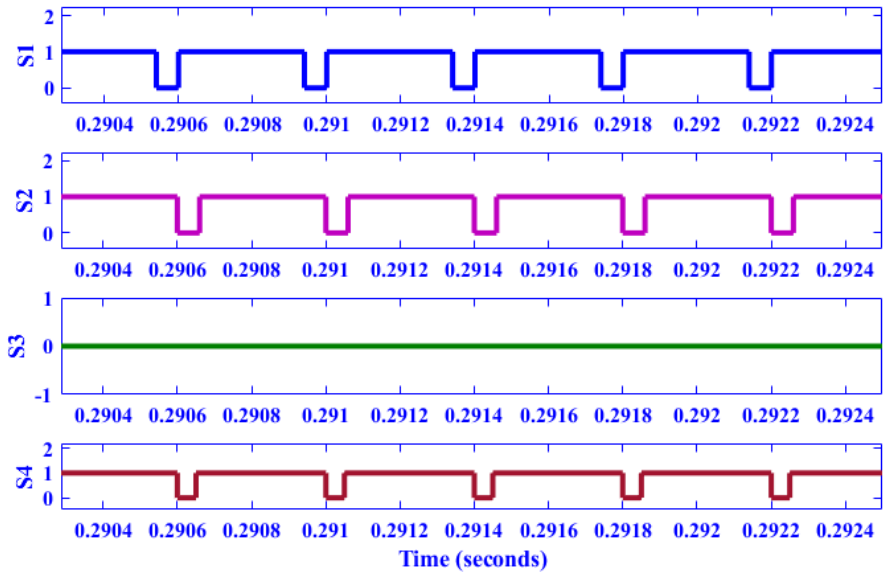


**Figure 4.9:** Simulated Gate Signals of the Switches for Operation Mode Three

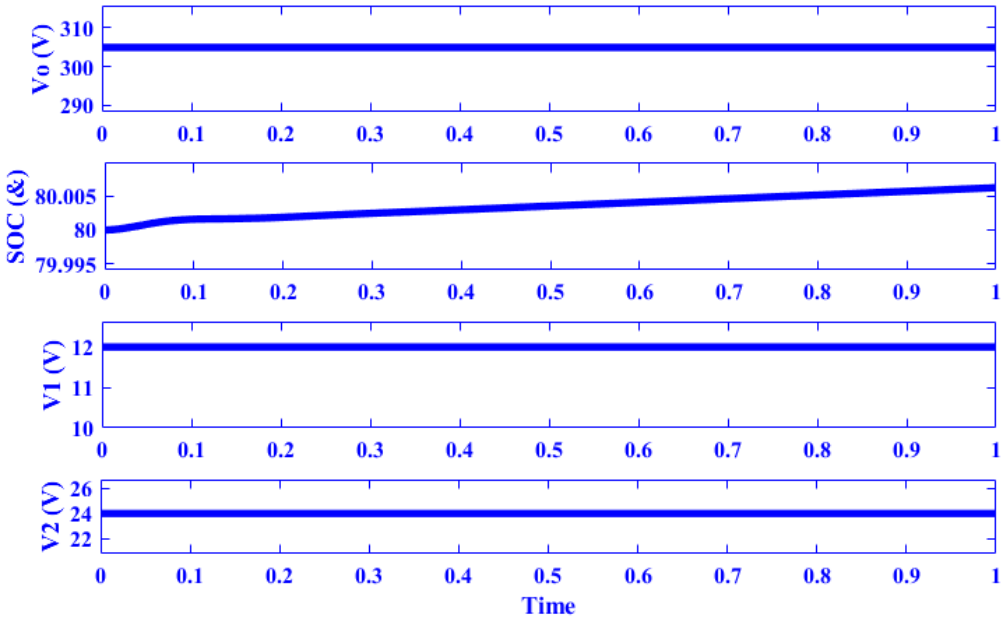


**Figure 4.10:** Voltage Levels and SOC Profile for Operation Mode Three

### 4.2.4 Open Loop Voltage Regulation of BITIHGC

The proposed BITIHGC has been tested during simulation to determine the feasibility of attaining different output voltages by varying the duty ratios. The voltage regulation is carried out in an open-loop mode without a controller. The voltage regulation results at 250 *V* and 300 *V* are shown in Figure 4.14, 4.15 and 4.16 respectively.

The rise time to about from 0 *V* to an overshoot of about 300 *V* in Figure 4.14 is 0.05 seconds. The settling time of the converter to the reference of 250 *V* is about 0.2 seconds. For the 300 *V* reference voltage in Figure 4.15, the overshoot hits 360 *V* before settling to 300 *V* in 0.24 seconds. These portray the capacity of the BITIHGC to regulate the output voltage level.

The very high overshoot and settling time is experienced when the reference voltage is 350 V as shown in Figure 4.16. The settling time of the converter to this reference value is about 0.4 seconds. The overshoot hits around 430 V before settling.

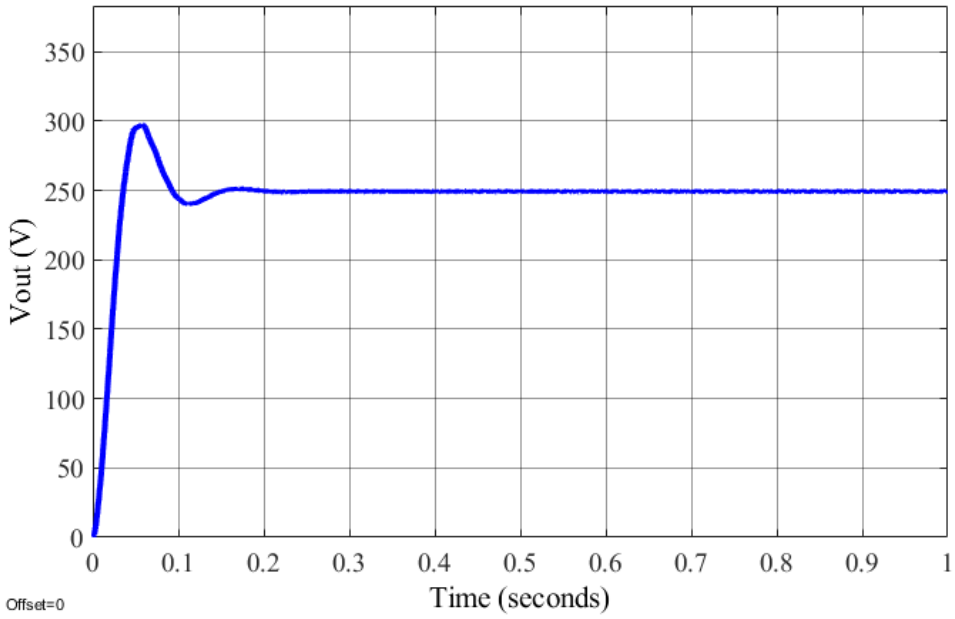


**Figure 4.11:** Open Loop Voltage Regulation Capability of the Proposed Converter when the Output Voltage is Commanded from 0 *V* to 250 *V*

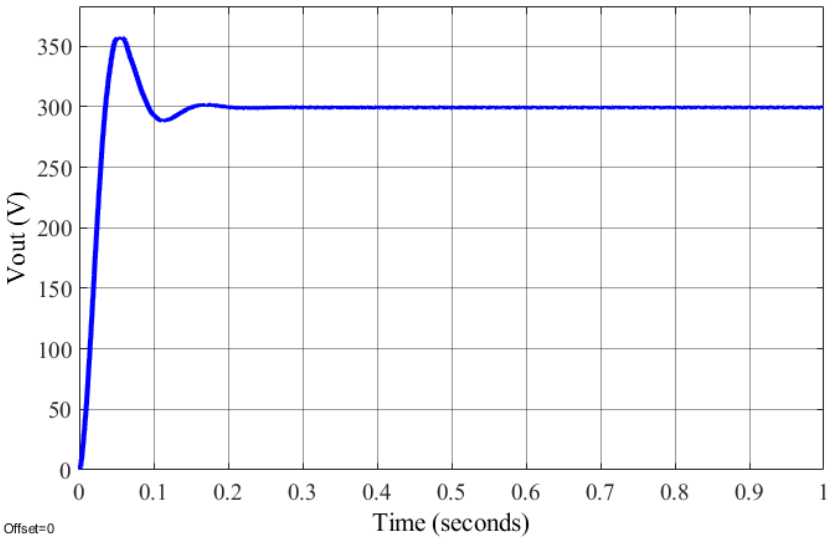


**Figure 4.12:** Open Loop Voltage Regulation Capability of the Proposed Converter when the Output Voltage is Commanded from 0 *V* to 300 *V*

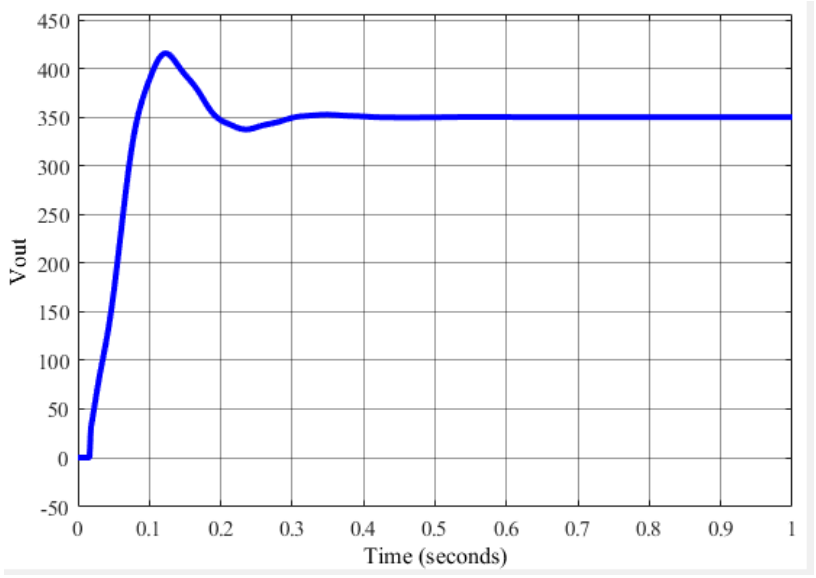


**Figure 4.13:** Open Loop Voltage Regulation Capability of the Proposed Converter when the Output Voltage is Commanded from 0 *V* to 350 *V*

### 4.2.5 Closed Loop Simulation Results

At this stage of the project, the performance of the controller is tested after implementation via simulations. The key performance indicators to be verified are the line regulation of the input sources, the regulation of the load to variations, and the capacity of

the converter to output the voltage as required. The results obtained will depict how the controller's dynamic response handles variations in reference voltage, input voltage levels, and load resistance.

### 4.2.6 Line Regulation Response during Operation Mode One

The simulation result in Figure 4.19 shows the waveform of the output voltage waveform when value of $V_1$ is stepped down from 12 $V$ to 6 $V$. There is no deviation from the output voltage of 300 $V$ as set by the reference voltage. The input current of the second input source, $I_{in2}$, increases to compensate for the power lost by the first input source. For another simulation conducted at same reference voltage of 300 $V$ with $V_2$ stepped down from 24 $V$ to 20 $V$, the output voltage is shown in Figure 4.20. The input current of the first input source, $I_{in1}$ increases as a measure to compensate for lost power by $V_2$. Also, no deviation is observed in the output voltage. In Figure 4.21, the reference voltage has been increased to 350 V. The step down of $V_2$ from 24 V to 18 V causes a small deviation in the output voltage. This occurs in the split time that the controller draws more power from the first input port, $V_1$ in order to compensate for the reduced power from $V_2$ at a higher load requirement.

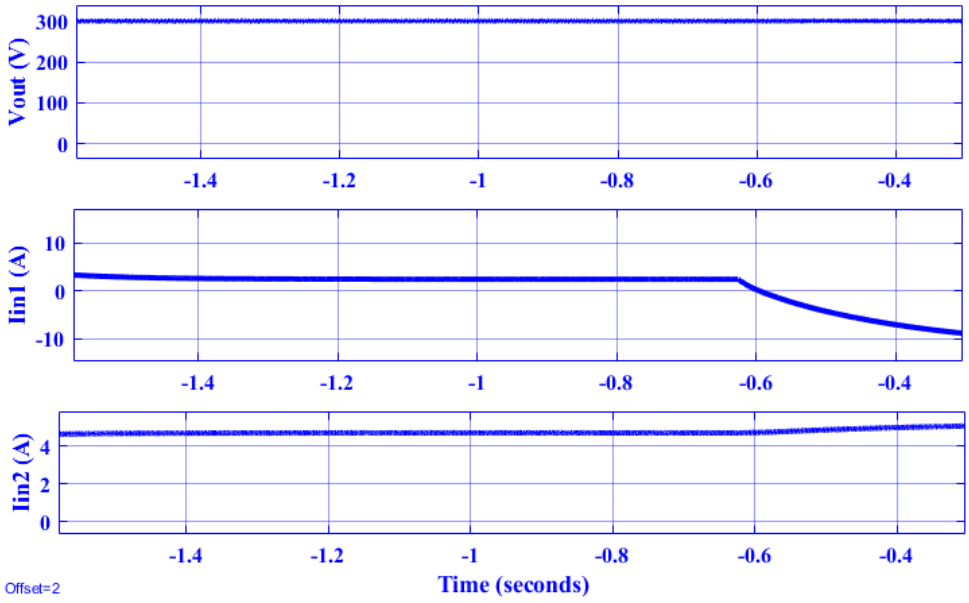


**Figure 4.14:** Simulated Line Regulation of the controller when $V_1$ is stepped down from 12 $V$ to 6 $V$ at 300 $V$ reference voltage

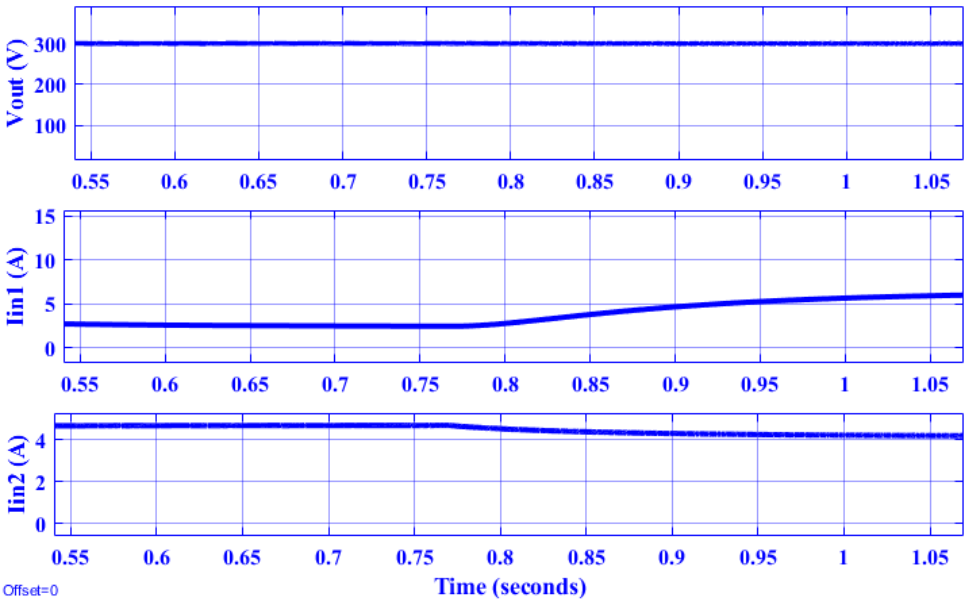


**Figure 4.15:** Simulated Line Regulation Response of the controller when $V_2$ is stepped down from 24 $V$ to 20 $V$ at 300 $V$ reference voltage

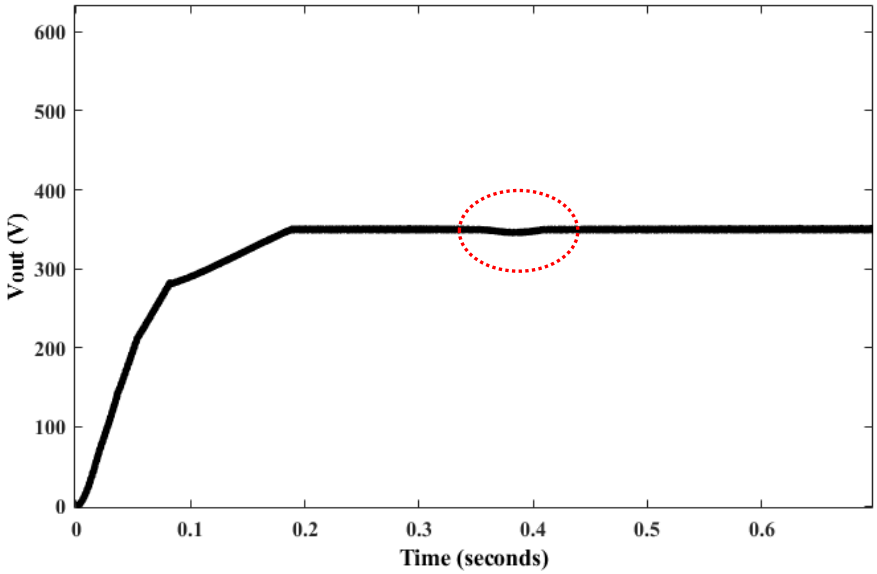


**Figure 4.16:** Simulated Line Regulation Response when $V_2$ Decreased to 18 *V* from 24 *V* at 350 *V* Output Voltage

### 4.2.7 Load Regulation Response During Operation Mode One

Figure 4.22 shows the behaviour of the output voltage when the load decreased from 1000 Ω to 500 Ω at a reference voltage of 350 *V*. Since the output power is incremented by two, the input power is also doubled. There are very small resulting transients in the output voltage.

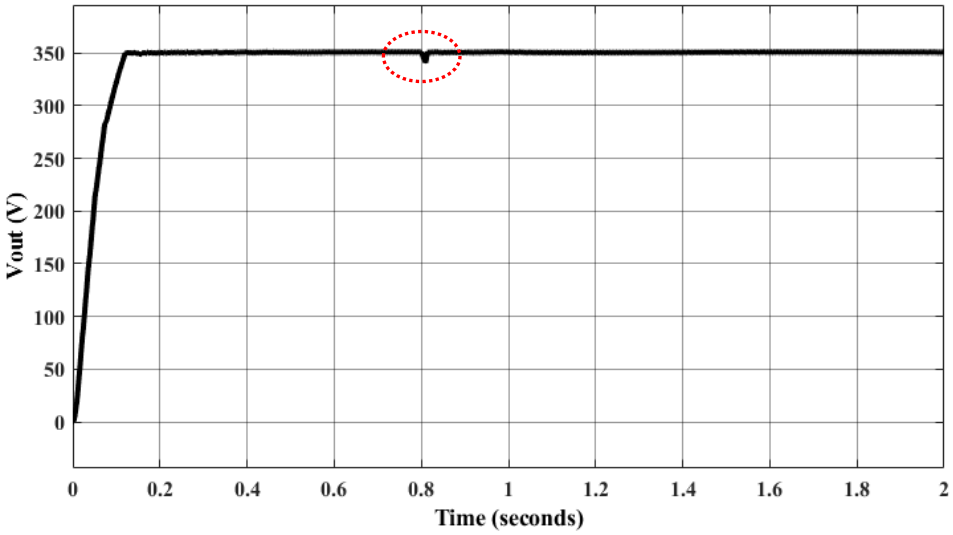


**Figure 4.17:** Simulated Load Regulation Response at Load of 500 Ω

### 4.2.8 Voltage Regulation Response During Operation Mode One

The initial tests for the voltage regulation, examined the ability of the controller to deliver a desired controlled voltage from a set reference voltage. At this stage, a single reference model is used. The response of the controller to different single reference voltages are depicted from Figures 4.23 to 4.25. The response at 250 *V*, 300 *V* and 350 *V* reference points are shown in Figures 4.23, 4.24 and 4.25 respectively.

From the schematics, it can be seen that the overshoot experienced during open loop simulation has been successfully eliminated by the controller. The controller is able to regulate the output voltage at 250 *V*, 300 *V* and 350 *V*, while maintaining a settling time of less than 0.2 seconds at the highest reference voltage.

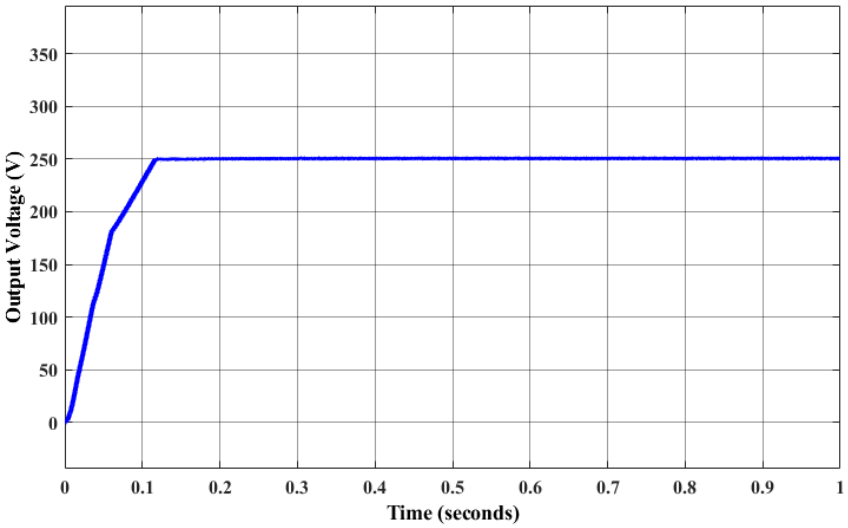


**Figure 4.18:** Simulated Voltage Regulation from 0 *V* to 250 *V*

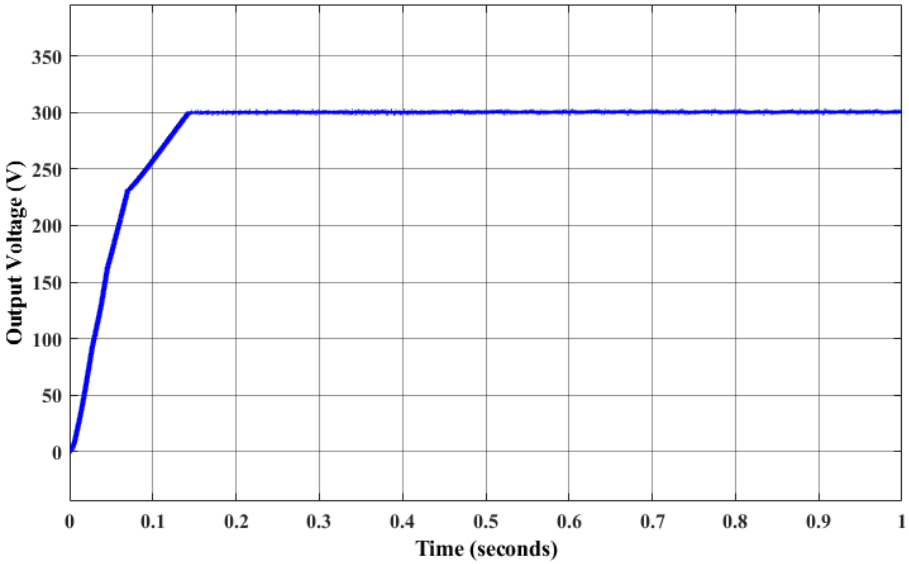


**Figure 4.19:** Simulated Voltage Regulation from 0 *V* to 300 *V*

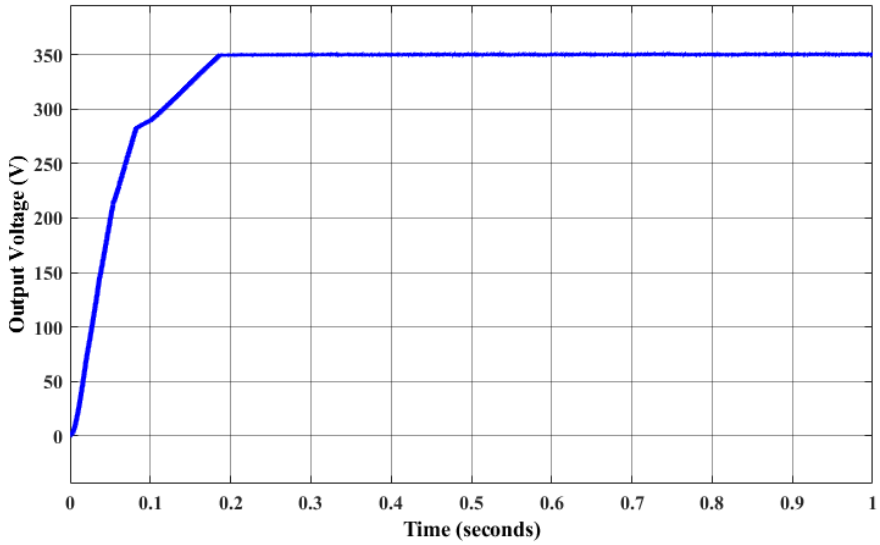


**Figure 4.20:** Simulated Voltage Regulation from 0 *V* to 350 *V*

The second stage of voltage regulation testing focused on testing multiple reference voltage points. The output voltage was manipulated to step up and step down arbitrarily by changing the reference voltage along the controller feedback path during simulation. The controller would then determine the duty ratios that correspond to the set reference voltage. The multi-reference simulation results are shown from Figures 4.26 to Figure 4.28. The

simulation results reveal that the output voltage transients have a very small rise time and an almost zero overshoot.

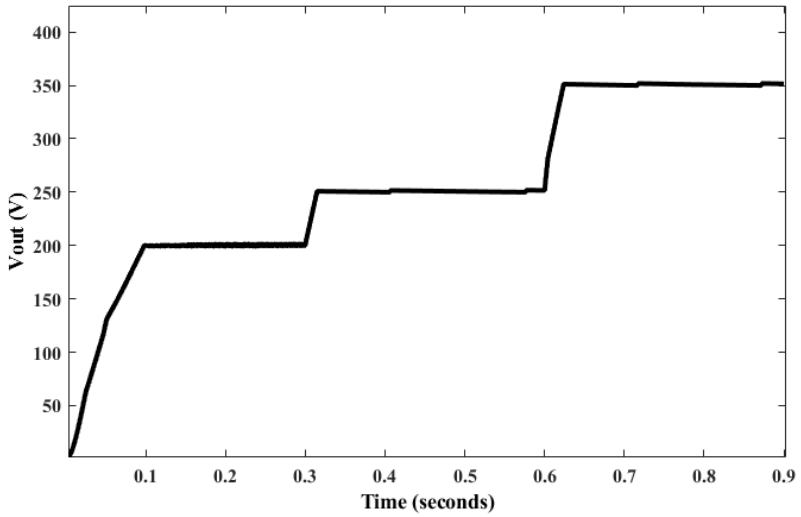


**Figure 4.21:** Simulated Dynamic Response from 0 *V* to 200 *V* to 250 *V* to 350 *V*

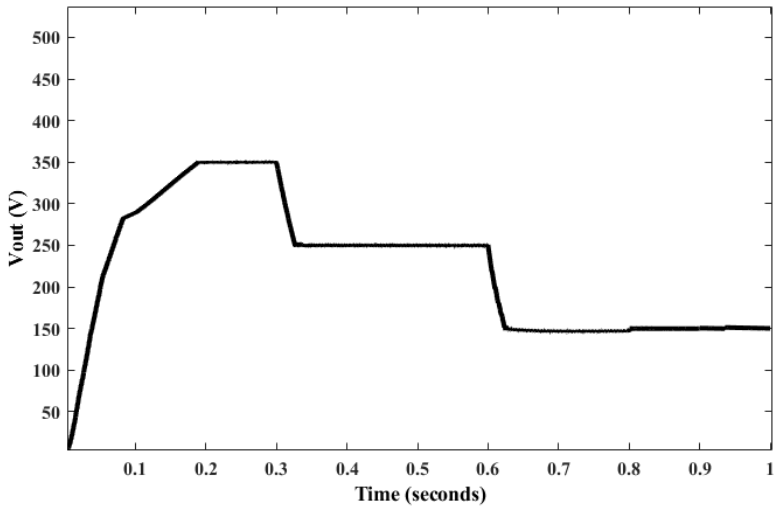


**Figure 4.22:** Simulated Dynamic Response from 0 *V* to 350 *V* to 250 *V* to 150 *V*

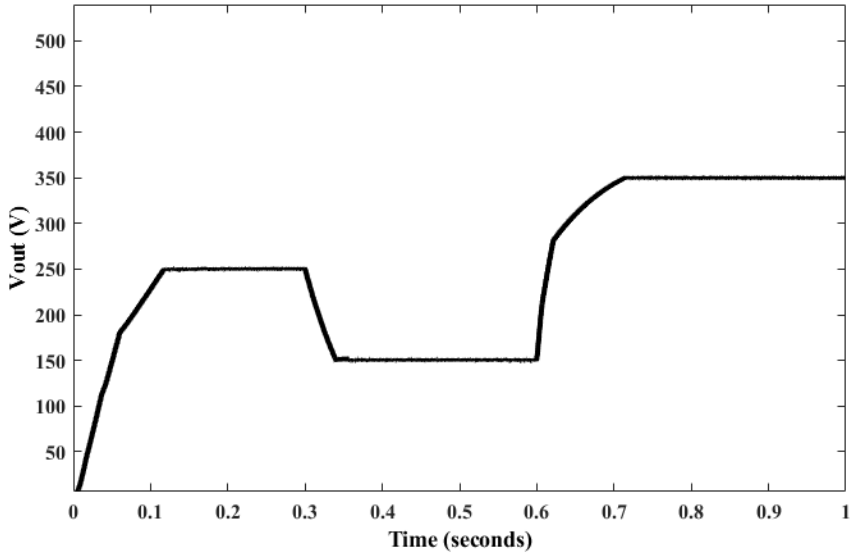


**Figure 4.23:** Simulated Dynamic Response from 0 *V* to 250 *V* to 150 *V* to 350 *V*

### 4.2.9 Voltage Regulation Response During Operation Mode Two

For the second operation mode, the input voltage of the two RE sources was set to 6 *V* each. The battery was primed at 12 *V*. Figure 4.24 shows the voltage regulation at 300 *V* single reference point. Despite the low input voltage, the controller is able to manipulate the battery to augment the RE input sources. A settling time of 0.35 seconds is achieved by the controller. Figure 4.25 shows the input/output voltages, battery current, and *SOC* levels of the battery. The battery *SOC* and current waveform confirm the depletion of the battery.

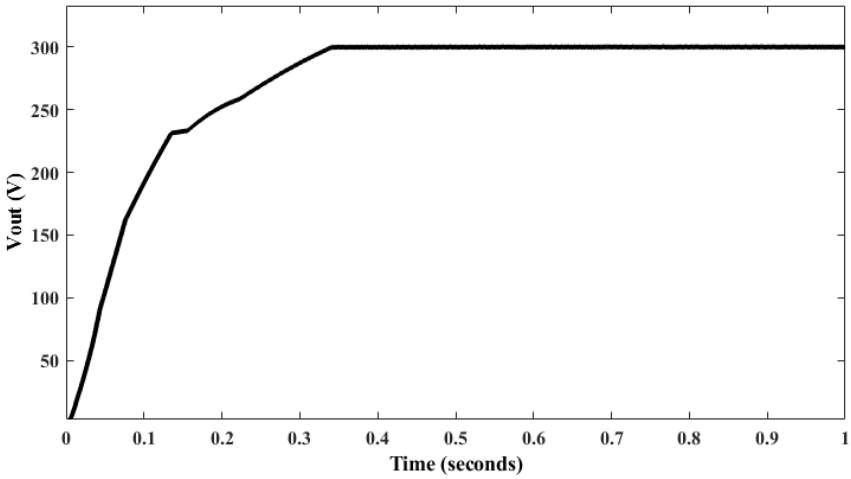


**Figure 4.24:** Simulated Voltage Regulation from 0 *V* to 350 *V* for Mode Two

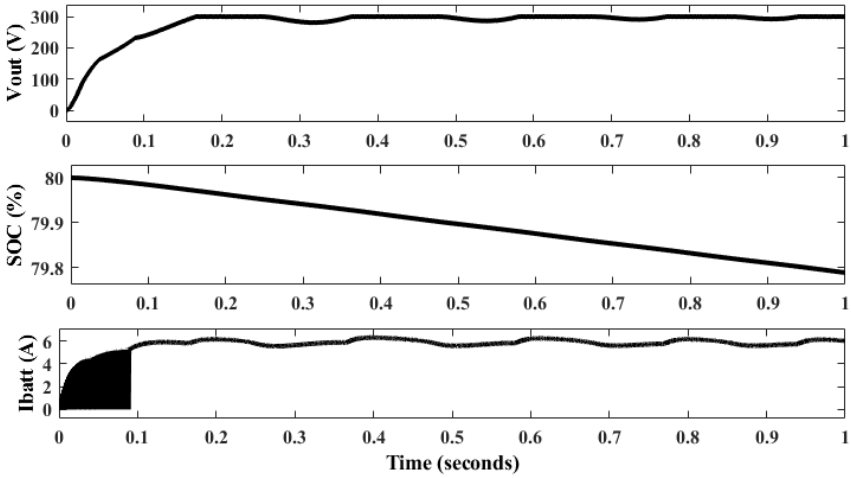


**Figure 4.25:** Simulated Output Voltage, SOC and Battery Current Levels during Mode Two

### 4.2.10 Voltage Regulation Response During Operation Mode Three

For the third operation mode, the load was reduced to 500 Ω while the input voltage of the two RE sources was set to the maximum 12 *V* and 24 *V* for $V_1$ and $V_2$ respectively. The battery *SOC* was reduced to 30 %. Figure 4.26 shows the input/output voltages, battery current, and *SOC* levels of the battery. The battery SOC and current waveform confirm the charging of the battery of the battery. The controller is able to deliver 300 *V* to the load while

charging the battery simultaneously. Comparing Figure 4.25 and Figure 4.26, it can be noticed that the output voltage during the second operation mode is not ripple free. This can be attributed to the tendency of the inductor current to enter the discontinuous conduction mode while the converter is battery fed.

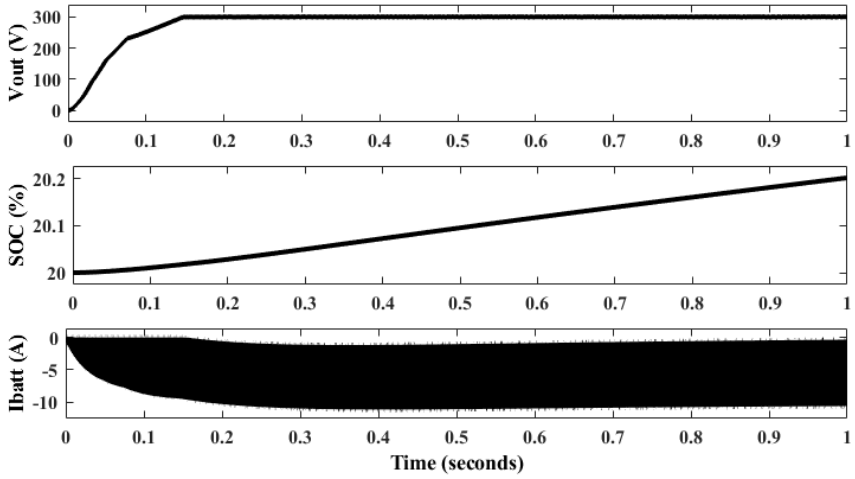


**Figure 4.26:** Simulated Output Voltage, SOC and Battery Current Levels during Mode Three

## 4.3 Open Loop Experimental Results

In order to confirm the accuracy of the theoretical and simulation results, tests were conducted in real time for the three operation modes. The same pattern of unmatched and matched input voltages was applied during tests. The results will be presented and discussed hereafter.

### 4.3.1 Open Loop Results for Operation Mode One

The gate signals fort this operation mode are depicted in Figure 4.27. The input voltage levels for this operation mode voltages; 12 *V* for $V_1$, and 24 *V* for $V_2$. The duty ratios were 75 % and 70 % for $d_1$ and $d_2$ respectively. The duty ratios of $S_3$ and $S_4$ were set to 50 %. Figure 4.28 shows the input and output voltage levels. The output voltage is about 315.53 *V*. The capacitor voltages, $V_{C1}$, $V_{C2}$ and $V_{C3}$ are displayed in Figure 4.29. The voltages are

127.19 $V$ for $V_{C2}$, and 139.54 $V$ for $V_{C3}$. The voltage on $C_1$, $V_{C1}$ is 266.69 $V$ and this is the sum of $V_{C2}$ and $V_{C3}$. This validates Equation 3.14 as derived. The capacitor, $C_1$ is idle during the first and fourth switching states as shown in Figure 4.30.

The waveforms of the inductor currents are presented in Figure 4.31. When $S_1$ and $S_2$ are conducting during the first switching state, currents $i_{L1}$ and $i_{L2}$ increase linearly as a result of $L_1$ and $L_2$ being charged by $V_1$ and $V_2$ respectively. A similar pattern is observed in $i_{L3}$ as $L_3$ is charged by $V_{C3}$. Inductor current, $i_{L1}$ decreases when $S_1$ is switched off in the second switching state while $i_{L2}$ and $i_{L3}$ continue increasing. Inductor currents, $i_{L2}$ and $i_{L3}$ linearly decrease with a negative slope during the third switching state when $S_2$ does not conduct while $i_{L1}$ increases for two consecutive switching states. The average inductor currents are approximately 2.12 $A$, 4.23 $A$ and 0.309 $A$ for $i_{L1}$, $i_{L2}$ and $i_{L3}$ respectively. The current ripples in Figure 4.31 are 18.4 %, 13.2 % and 25.7 % for $i_{L1}$, $i_{L2}$ and $i_{L3}$ respectively. These high current ripples can be attributed to non-ideal components, absence of a snubber or improper oscilloscope tuning.

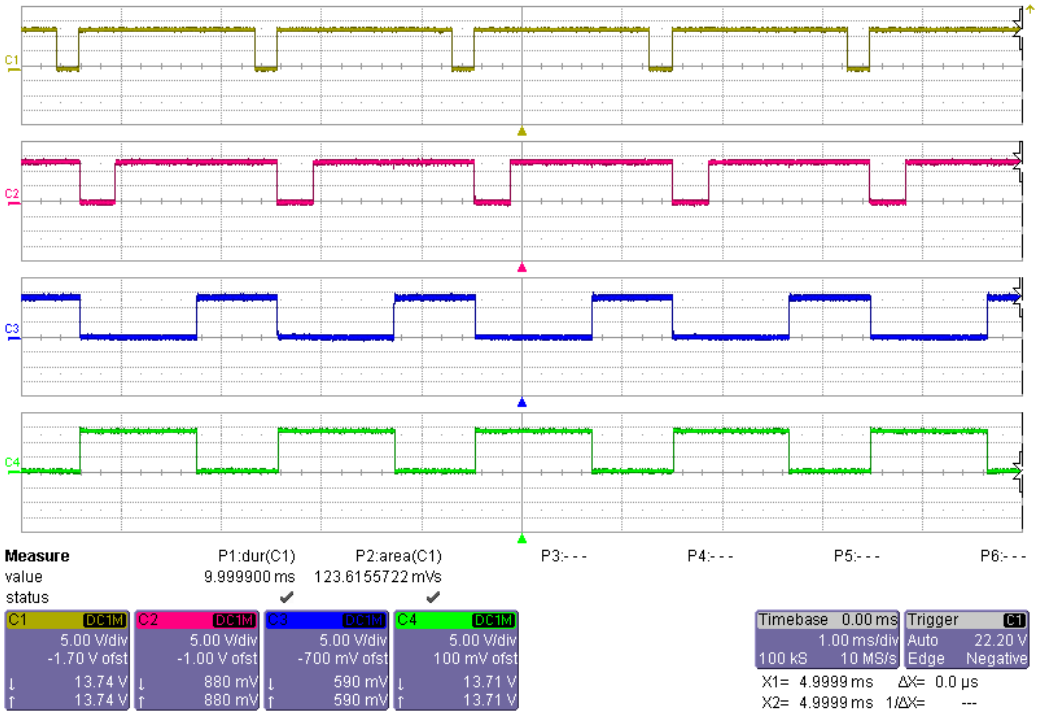


**Figure 4.27:** Experimental Gate Pulses of Switches $S_1$, $S_2$, $S_3$ and $S_4$ for Operation Mode One (CH1, CH2, CH3 and CH4)[$d_1$=75%; $d_2$=70%; $d_3 = d_4$ =50%]

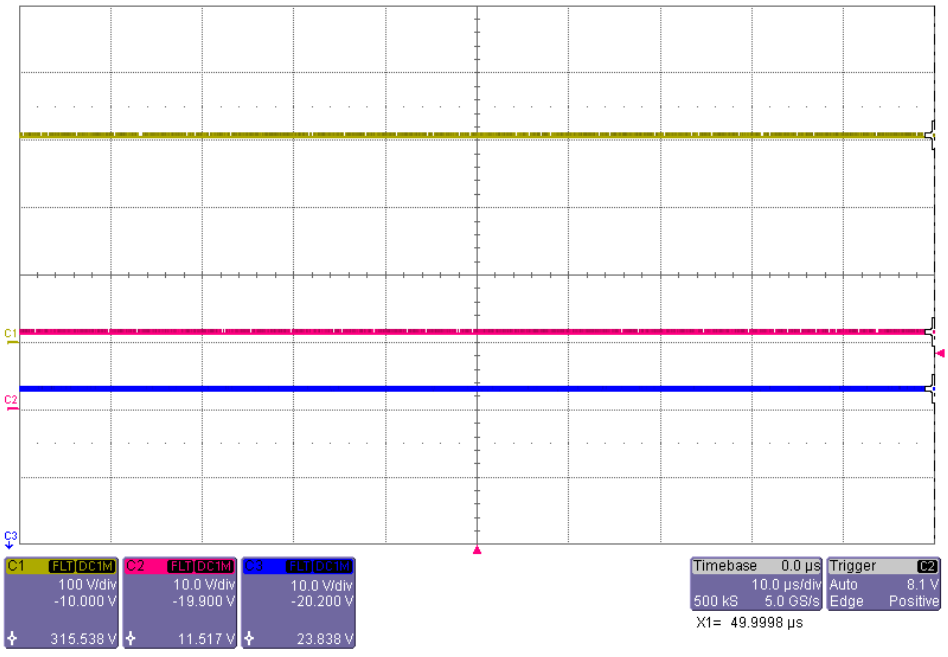


**Figure 4.28:** Output Voltage $V_{out}$ (CH1); Input Voltages $V_1$ and $V_2$ (CH2 and CH3)

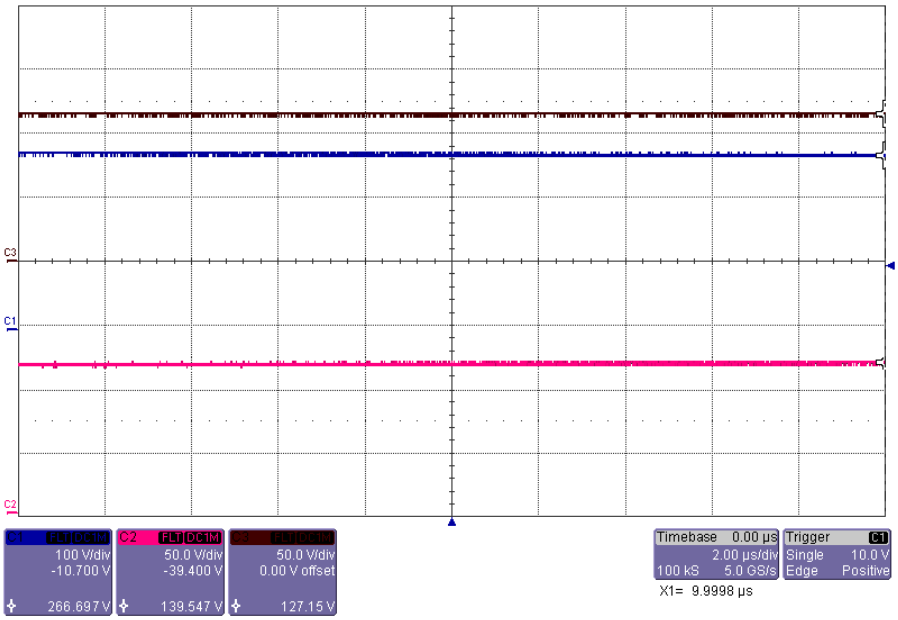


**Figure 4.29:** Capacitor Voltages $V_{C1}$, $V_{C3}$ and $V_{C2}$ (CH1, CH2 and CH3) for Mode One

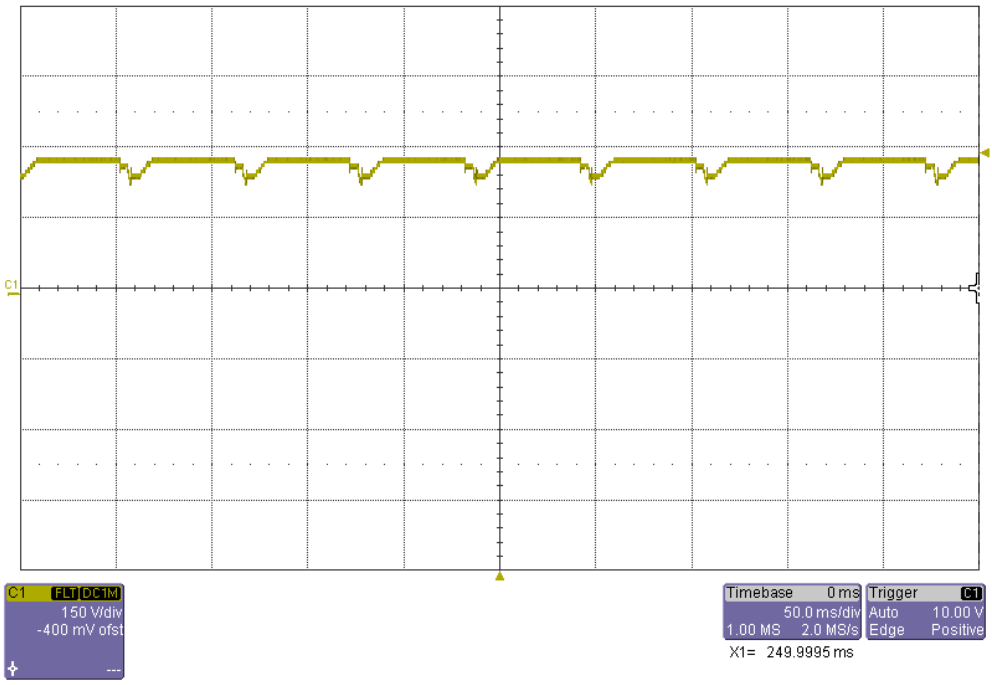


**Figure 4.30:** Capacitor Voltage Waveform $V_{C1}$

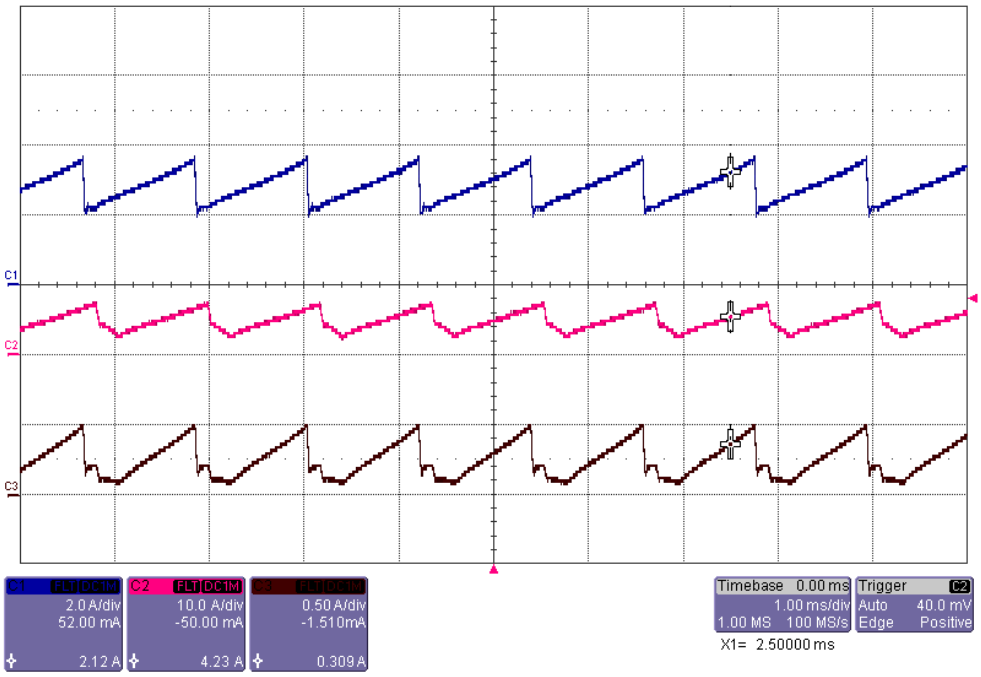


**Figure 4.31:** Inductors Current $I_{L1}$, $I_{L2}$ and $I_{L3}$ (CH1, CH2 and CH3) for Operation Mode One

The voltage stress of the switches, $S_1$ and $S_2$ is shown in Fig 4.32. It can be observed that the appearance of the voltage across $S_1$ occurs during the second switching state and during switching state three for $S_2$. The voltage stresses, $V_{S1}$ and $V_{S2}$, across $S_1$ and $S_2$ are about 64.87 $V$ and 119.54 $V$ respectively. These waveforms concur with the simulation result and validate Equation 3.2 and Equation 3.7 respectively. For $V_{S3}$ and $V_{S4}$, the voltage stress is 0.8 $V$ as depicted in Figure 4.33 and tallies with the theoretical and simulation result.

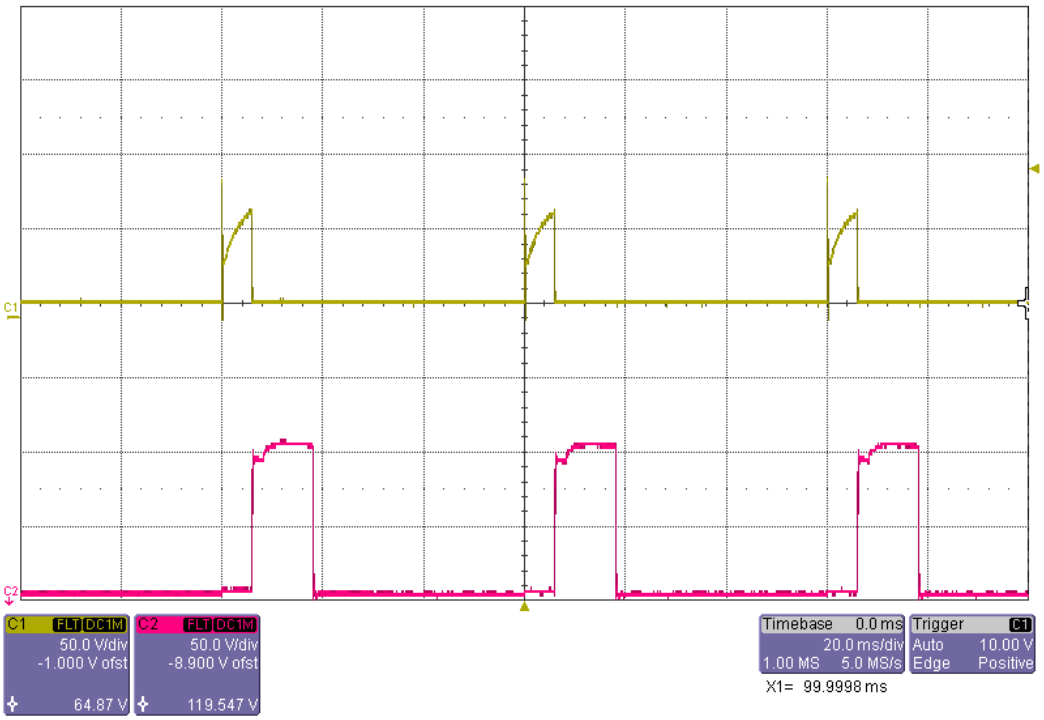


**Figure 4.32:** Switch Voltage $V_{S1}$ and $V_{S2}$ (CH1 and CH2) for Mode One

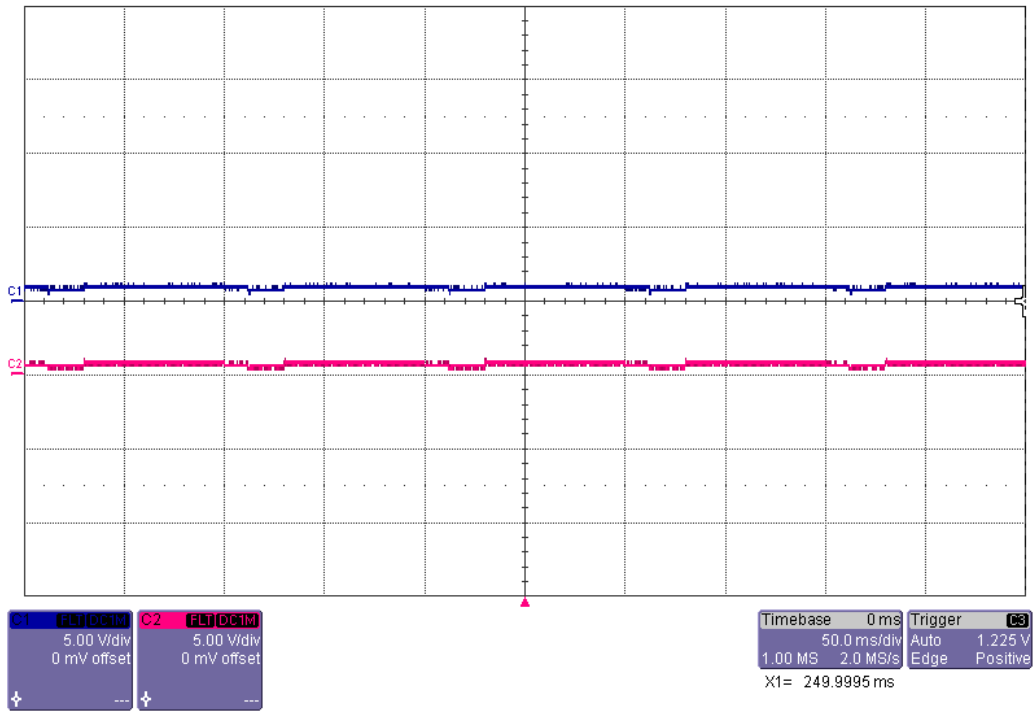


**Figure 4.33:** Switch Voltage $V_{S3}$ and $V_{S4}$ (CH1 and CH2) for Mode One

### 4.3.2 Open Loop Results for Operation Mode Two

The waveforms of gate signals for this operation mode are presented in Figure 4.34. It can be noticed that switch, $S_3$ is permanently turned on. The input voltage levels during this operation mode have been decreased to 6 *V* for $V_1$, and 12 *V* for $V_2$. The battery voltage is 12 *V*. Duty ratios of 75 %, 70 %, and 75 % for $d_4$, $d_2$ and $d_1$ were applied. Figure 4.45 shows these input and output voltage levels. The output voltage is about 311.57 *V*. The waveforms of the inductor currents ($i_{L1}$, and $i_{L2}$) are shown in Figure 4.36. The current ripples in Figure 4.36 are 24.3 %, and 21.7 % for $i_{L1}$ and $i_{L2}$ respectively. Better current ripples can be by including the snubber circuit or tuning the oscilloscope.

The voltage stress on $S_3$ and $S_4$ are shown in Figure 4.37. The voltage stress on $S_4$, $V_{S4}$ is equal to the battery supply voltage, $V_b$ = 12 *V*. The voltage stress on $S_3$, $V_{S3}$ is the forward voltage of 0.8 *V*. Figure 4.38 displays the battery current. The battery current rises to about 5.49 *A* during the first three switching states and reduces in the last switching state. The value of $i_b$ is the product of the duty ratio of switch, $S_4$ by the summation of the inductor currents.

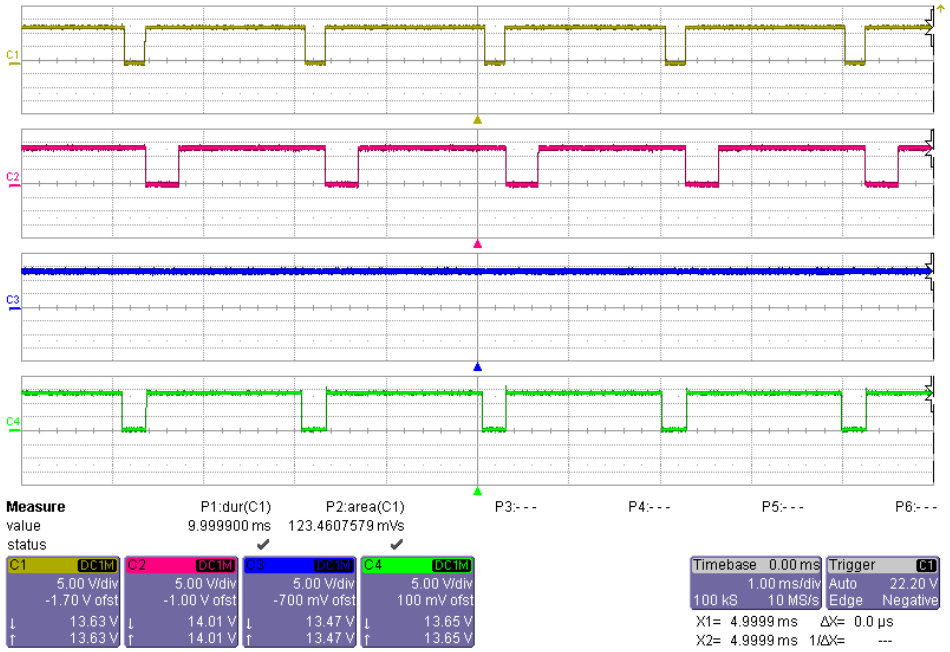


**Figure 4.34:** Experimental Gate Pulses of Switches $S_1$, $S_2$, $S_3$ and $S_4$ for Operation Mode Two (CH1, CH2, CH3 and CH4)[$d_1 = d_4 = 75\%$; $d_2 = 70\%$; $d_3 = 50\%$]

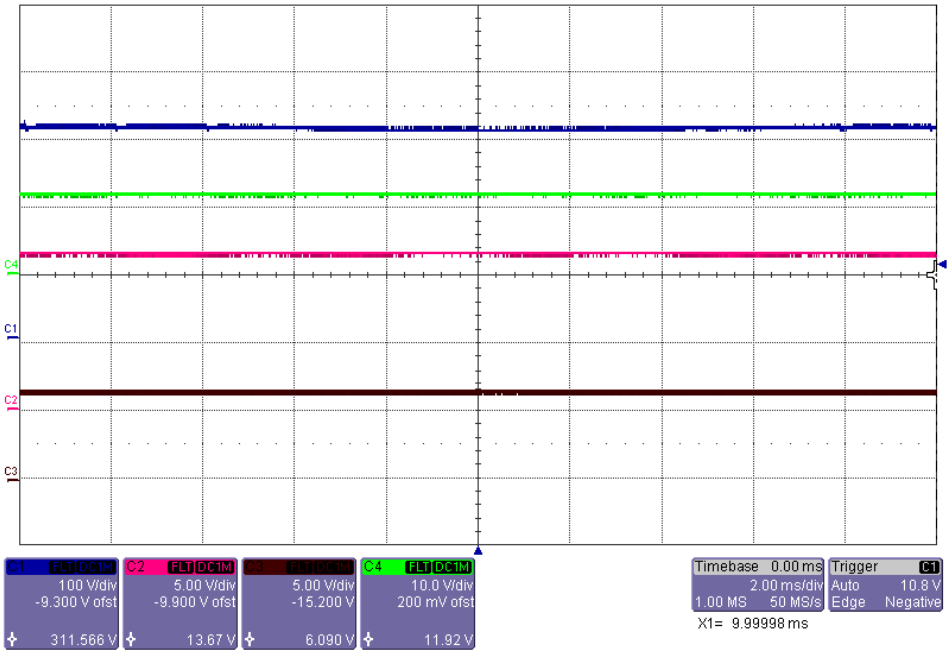


**Figure 4.35:** Output Voltage $V_{out}$ (CH1); Input Voltages $V_1$ and $V_2$ (CH2 and CH3); Battery Voltage $V_b$ (CH4) for Operation Mode Two

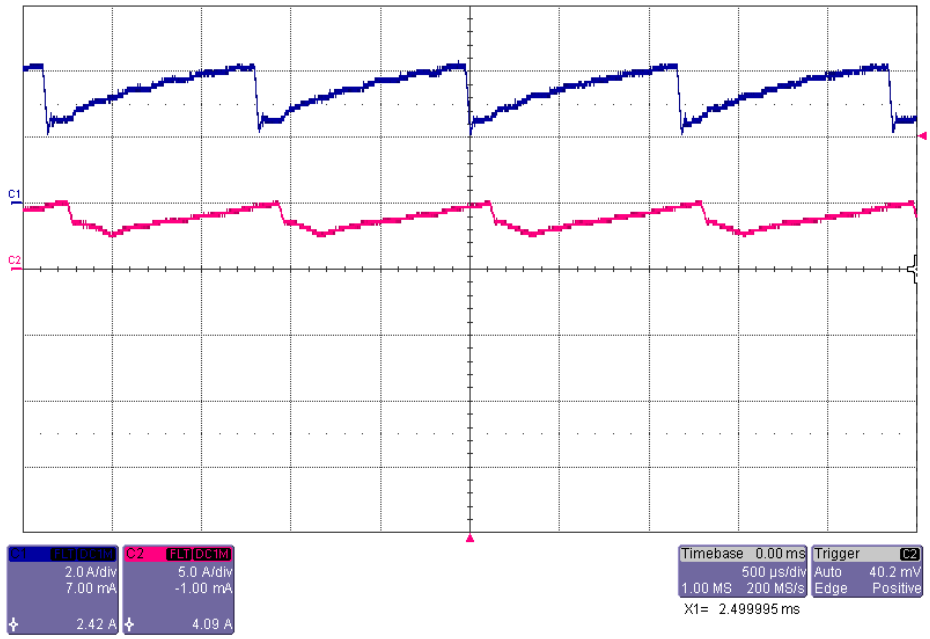


**Figure 4.36:** Inductors Current $I_{L1}$ and $I_{L2}$ (CH1 and CH2) for Operation Mode Two

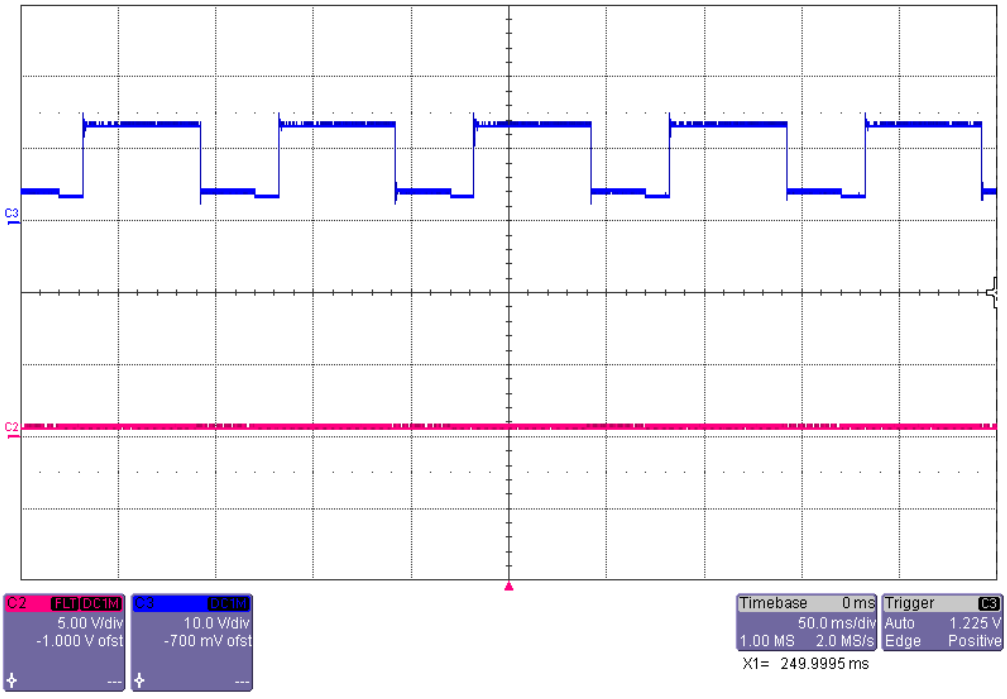


**Figure 4.37:** Switch Voltage $V_{S3}$ and $V_{S4}$ (CH2 and CH3) for Mode Two

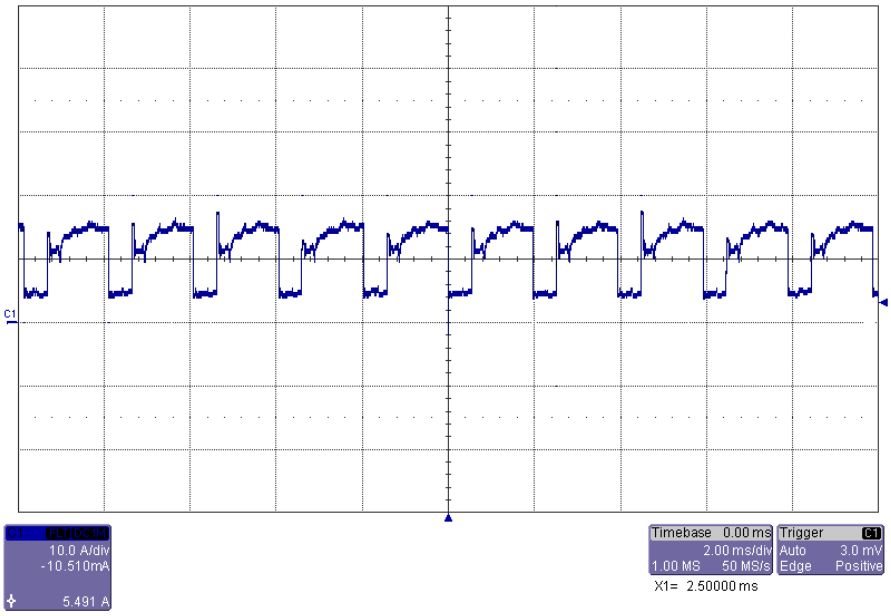


**Figure 4.38:** Battery Current $i_b$ for Operation Mode Two

### 4.3.3 Open Loop Results for Operation Mode Three

The waveforms of gate signals generated for the third operation mode are presented in Figure 4.39. It can be observed that switch, $S_3$ is permanently turned off. The input voltage levels during this operation mode are 12 $V$ for $V_1$, and 24 $V$ for $V_2$. Duty ratios of 0.75, and 0.7 have been applied for $d_1$ and $d_2$. The duty ratio for $d_4$ is set to 0.75. Figure 4.40 shows the output voltage, and the voltage on $C_1$. The measured output voltage is about 301.32 $V$. The voltage on $C_1$ is about 277.69 $V$. While the converter serves the load, the battery is charged during the third switching state when there is a negative slope on the signal.

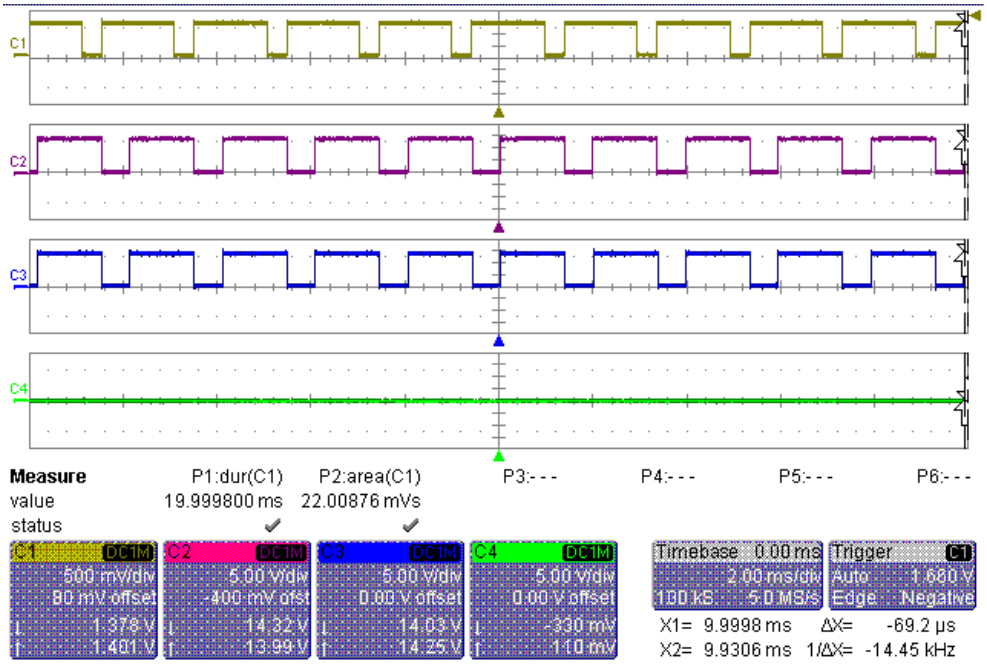


**Figure 4.39:** Experimental Gate Pulses of Switches $S_1$, $S_2$, $S_3$ and $S_4$ for Operation Mode Three (CH1, CH2, CH4 and CH3)[$d_1$= 75%; $d_2$ = 70%; $d_3$ = 50%; $d_4$ = 65%]

The voltage stress on $S_3$ and $S_4$ is depicted in Figure 4.41. $V_{S3}$ goes to zero in the third switching state and returns to about 10 $V$ which is the voltage of the depleted battery. A voltage spike can be observed in $V_{S3}$. This voltage spike occurs during switching state 3 when turning off $S_3$ and $S_4$ forces the current to charge the $V_b$ through diodes, $D_{b1}$ and $D_{b2}$. The current of the inductors and battery is shown in Figure 4.42. It indicates the spike in the battery current when $D_{b1}$ and $D_{b2}$ conduct. The current ripples in Figure 4.42 are 29.2 % and 26.3 % for $i_{L1}$, and $i_{L2}$ respectively. Comparing the current ripples in the different operation modes, it can be observed that the highest current ripple occurred during the third operation mode. This may be attributed to AC currents associated to the battery charging and load. A larger output capacitor would ameliorate the problem.

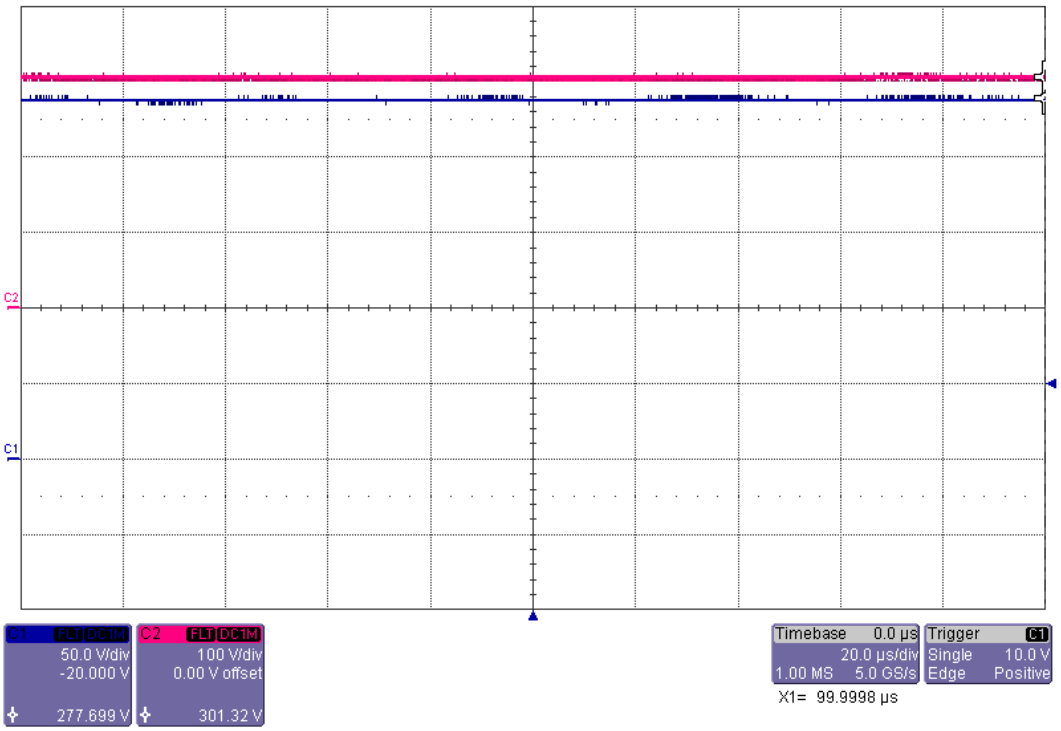


**Figure 4.40:** Capacitor Voltage $V_{C1}$ (CH1) and Output Voltage $V_{out}$ (CH2) for Operation Mode Three

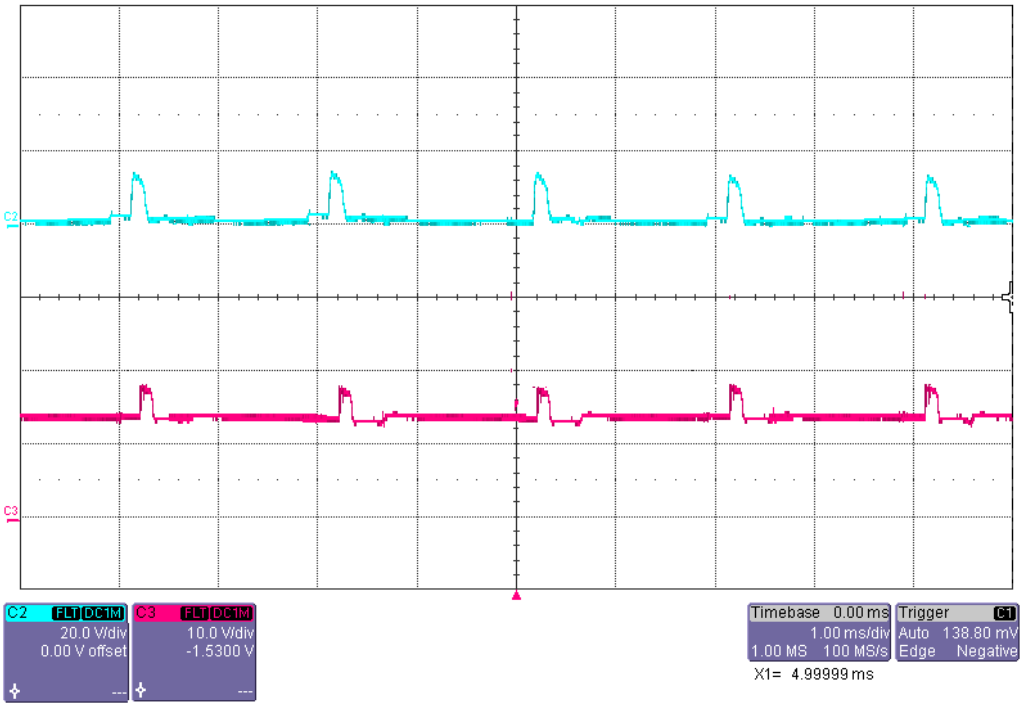


**Figure 4.41:** Switch Voltage $V_{S3}$ and $V_{S4}$ (CH2 and CH3) for Operation Mode Two

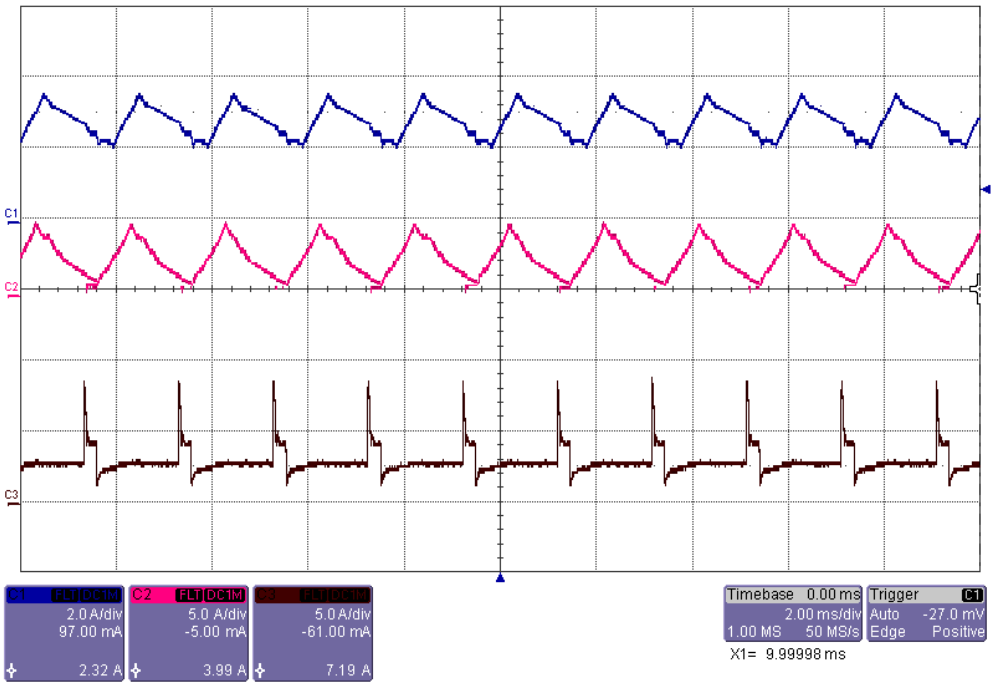


**Figure 4.42:** Inductors and Battery Current $I_{L1}$, $I_{L2}$ and $i_b$ (CH1, CH2 and CH3) for Operation Mode Three

### 4.3.4 Open Loop Voltage Regulation Results

The experimental output voltage regulation tests were carried out in open loop mode to check the response of the proposed converter to change in duty ratio during the primary operation mode. The variation of the duty ratio was done on the ControlDesk interface. The voltage regulation result at 200 *V* is presented in Figure 4.43. For 250 *V* reference voltage, the result can be seen in Figure 4.44 while and that of 350 *V* is shown in Figure 4.45. The results have shown that the proposed three-input converter can regulate the output voltage at 200 *V*, 250 *V* and 350 *V*. Also, the transients in output voltage transient possess a minimal overshoot, and a short rise time. These tally with the dynamic response during simulation.

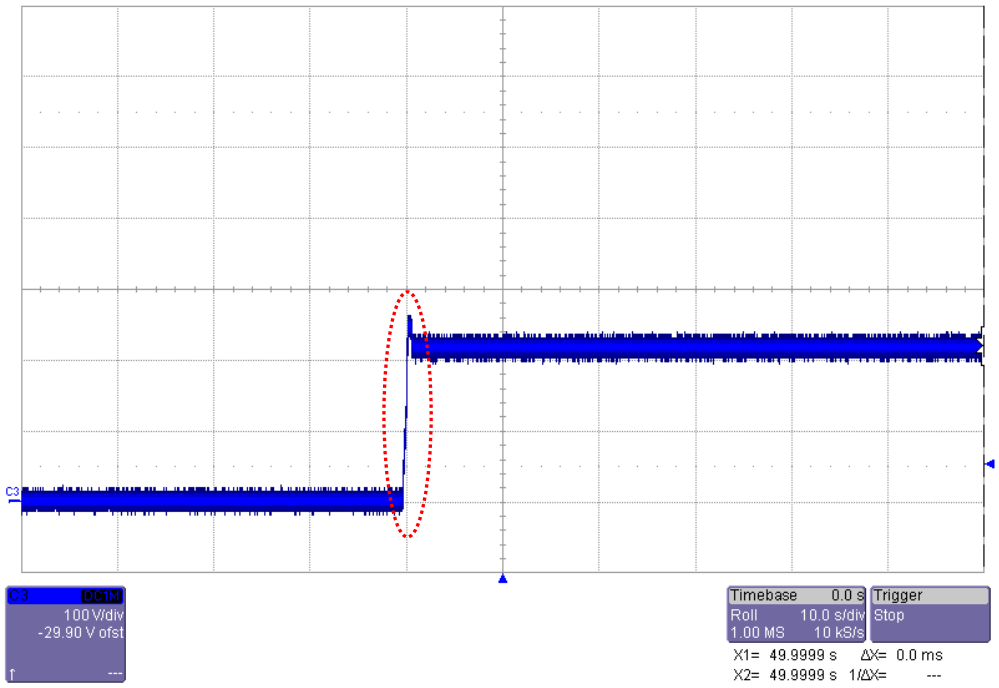


**Figure 4.43:** Experimental Open Loop Voltage Regulation from 0 *V* to 200 *V*

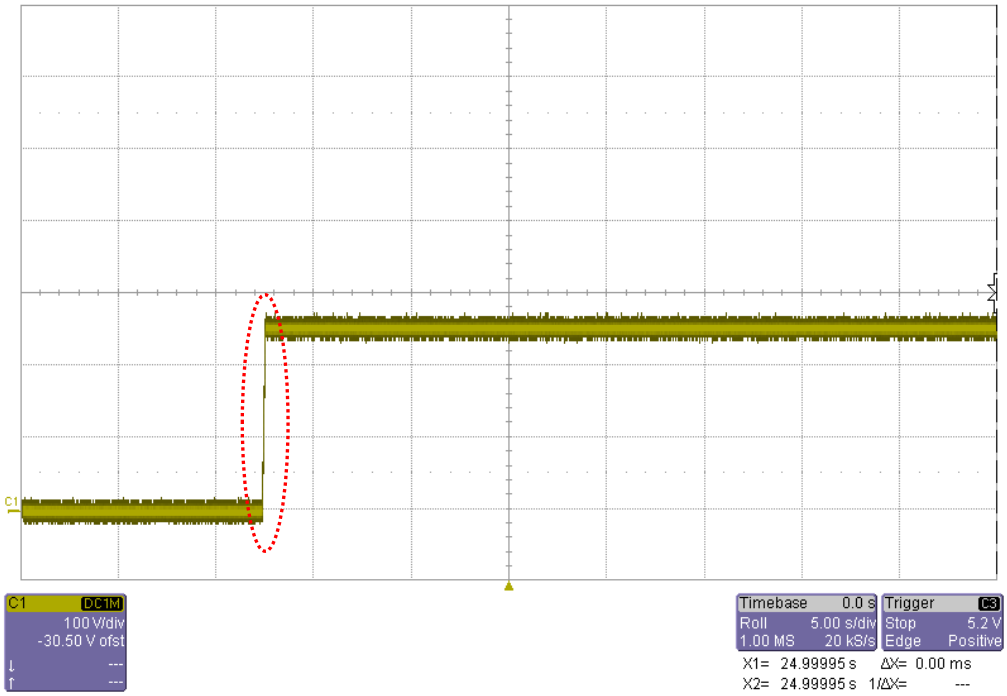


**Figure 4.44:** Experimental Open Loop Voltage Regulation from 0 *V* to 250 *V*

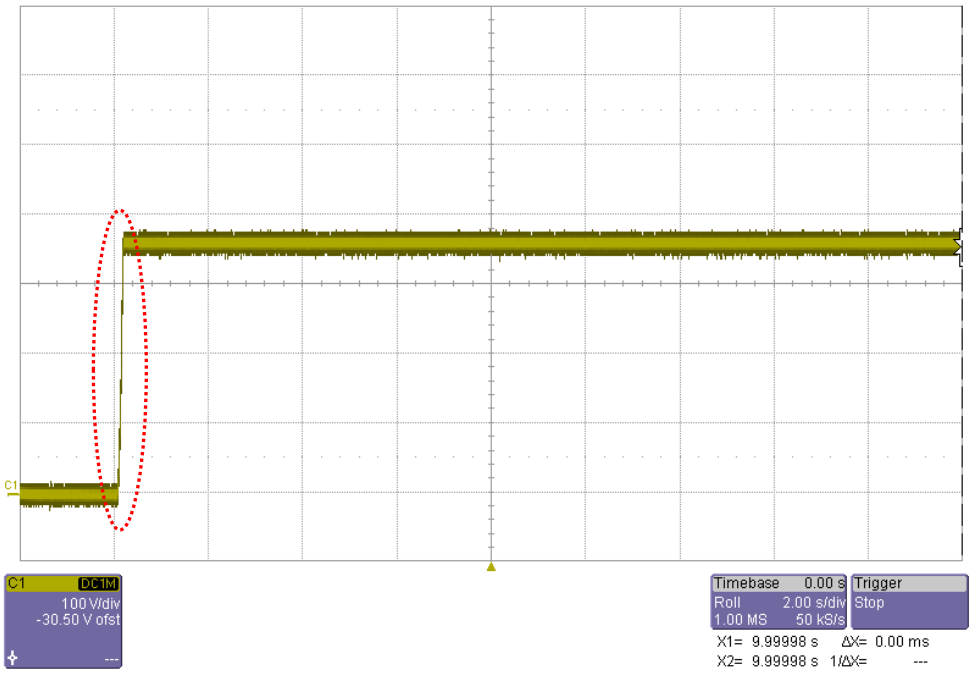


**Figure 4.45:** Experimental Open Loop Voltage Regulation from 0 *V* to 350 *V*

## 4.4 Closed Loop Experimental Results

In conducting the closed loop experiments, the proposed ANN controller has been implemented. The tests are performed on the closed-loop converter circuit. The key indicators are the dynamic response to hardware changes in reference voltage, input voltage levels, and load resistance.

### 4.4.1 Line Regulation Response

Figure 4.46 shows the output voltage waveform and average value of the input currents experimental results showing dynamic response of the proposed three-input boost converter when $V_1$ is decreased to 9 *V* and $V_2$ is decreased to 18 *V*. While there is small deviation from the desired output voltage for a split microsecond, the controller is able to return to delivering the voltage as required. The average current drawn from the input source $V_2$ is increased when that of $V_1$ drops.

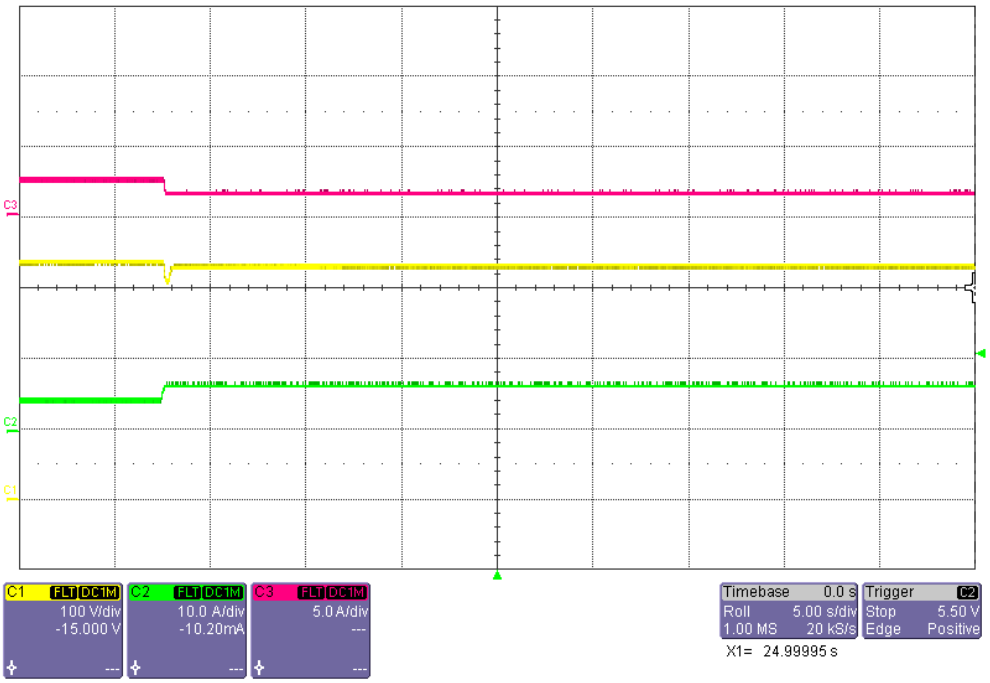


**Figure 4.46:** Line Regulation Response

### 4.4.2 Load Regulation Response

Figure 4.47 shows the output voltage waveform when the load requirement is decreased to 800 Ω. It can be seen that the current is drawn from the two input sources. The transients are negligible.

### 4.4.3 Voltage Regulation Response

The single reference point testing for the voltage regulation of the proposed converter is presented. Figure 4.48 shows the capacity of the controller to regulate the output voltage at 250 *V*, Figure 4.49 presents that for 300 *V* while Figure 4.50 depicts the response when the output is stepped up from zero volts to 350 *V*. Overshoots have been eliminated by the controller and there is a short rise time by the waveforms.

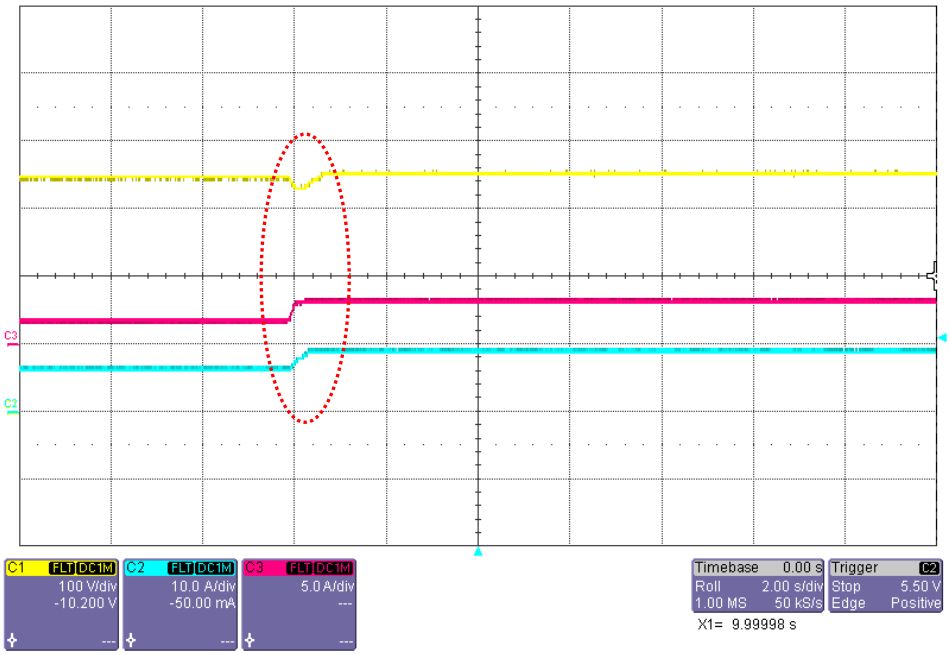


**Figure 4.47:** Load Regulation Response

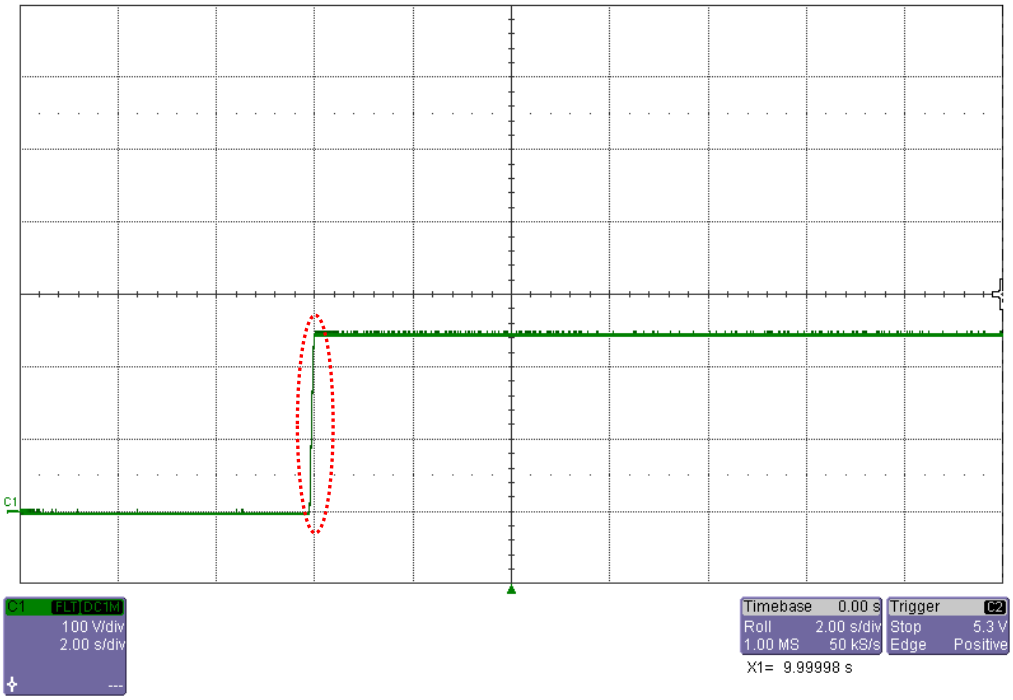


**Figure 4.48:** Voltage Regulation from 0 *V* to 250 *V*

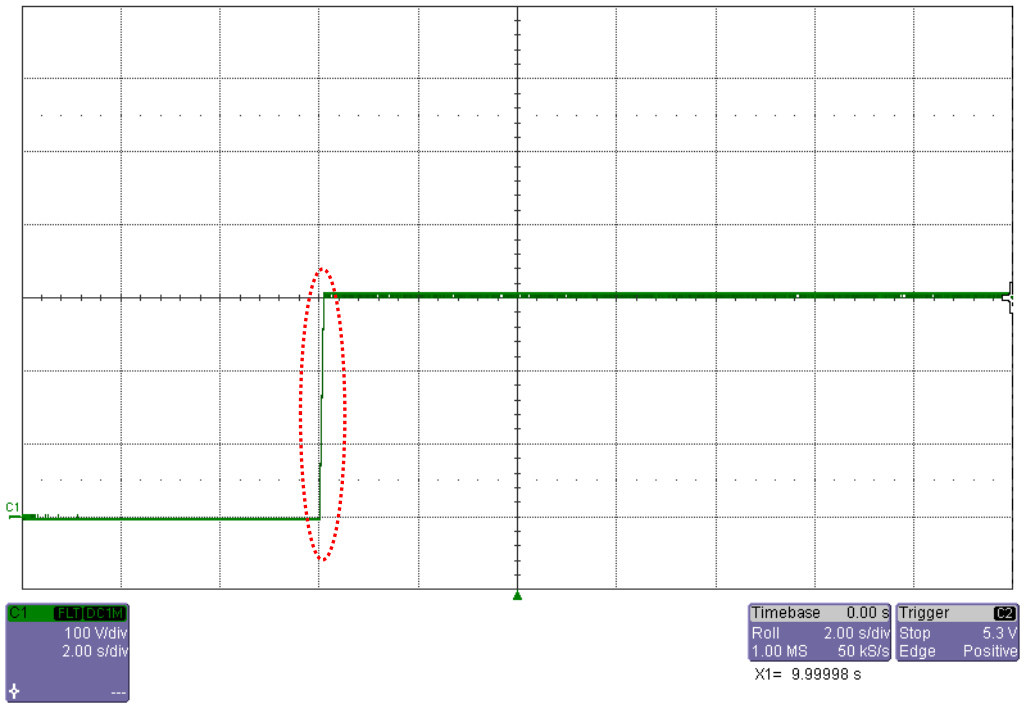


**Figure 4.49:** Voltage Regulation from 0 *V* to 300 *V*

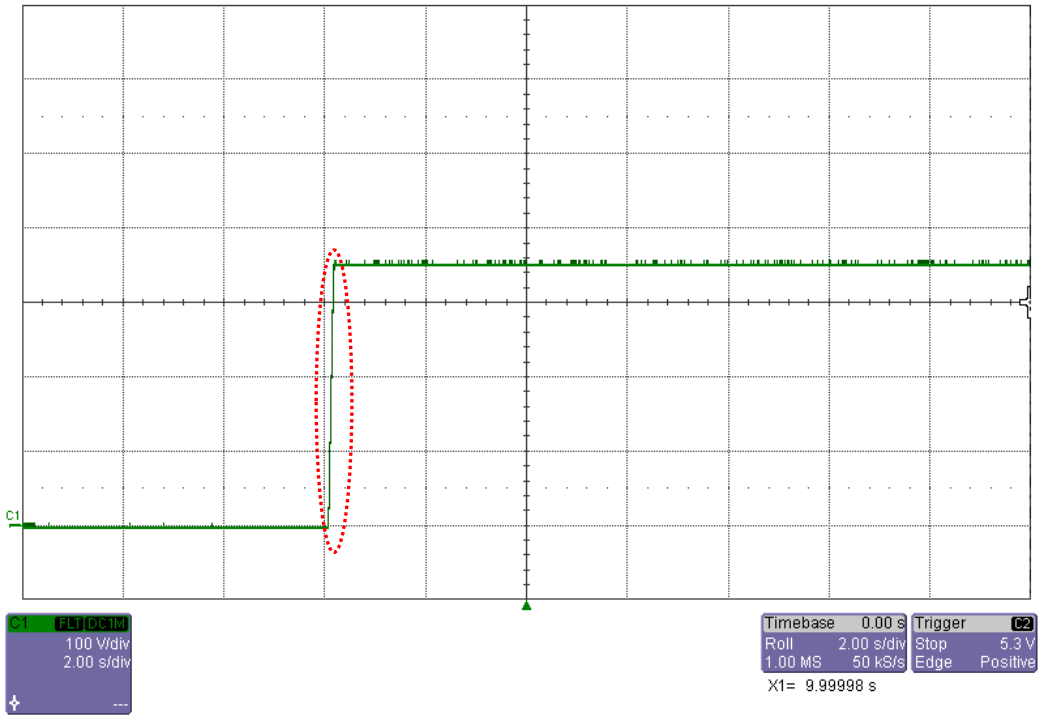


**Figure 4.50:** Voltage Regulation from 0 *V* to 350 *V*

For the multi-reference closed loop voltage regulation, under different cases and different output voltage values, the results of arbitrary output voltage when manipulated to step up and down are shown from Figure 4.51 up to Figure 4.53.

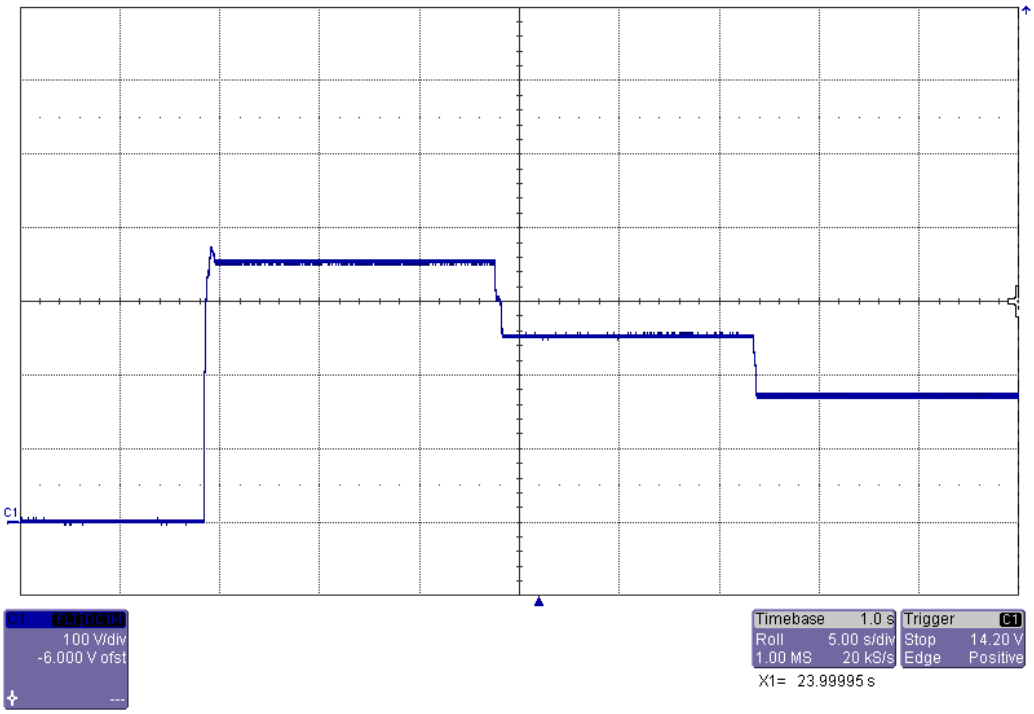


**Figure 4.51:** The Dynamic Response from 0 *V* to 350 *V* to 250 *V* to 180 *V*

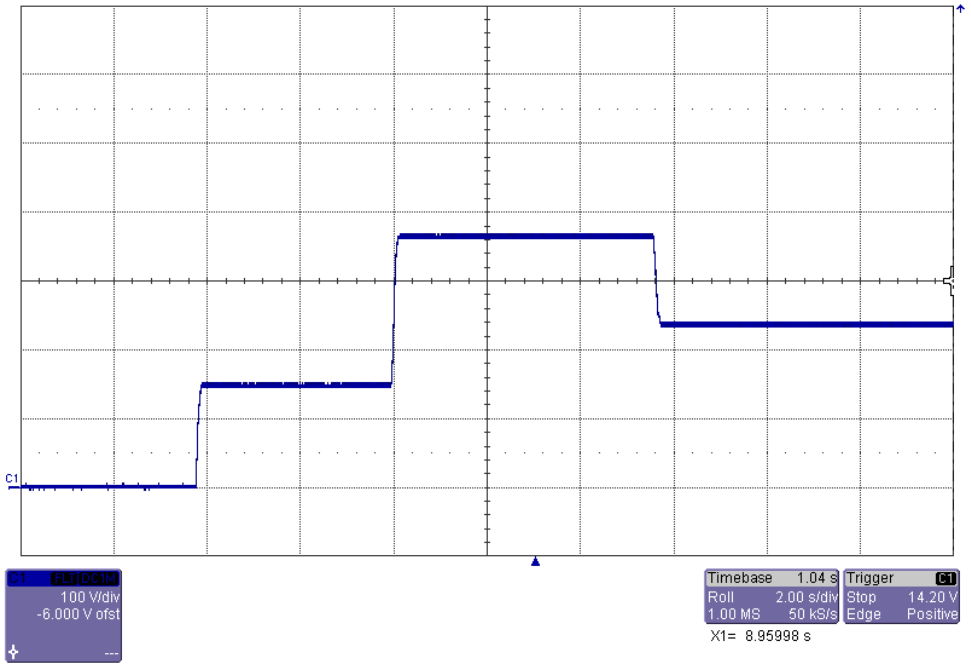


**Figure 4.52:** The Dynamic Response from 0 *V* to 150 *V* to 350 *V* to 250 *V*

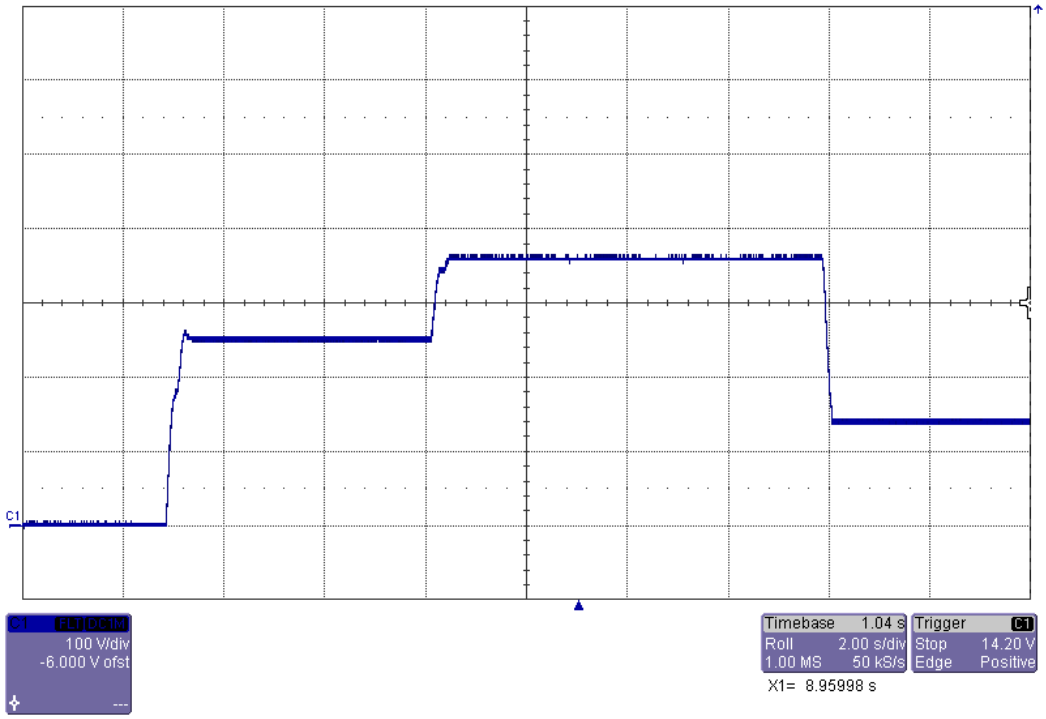


**Figure 4.53:** The Dynamic Response from 0 *V* to 250 *V* to 350 to 150 *V*

## 4.5 Performance Analysis and Comparisons

The major advantage of the boost / non-coupled inductors approach, adopted in the proposed three input converter is the high voltage gain. In this section, comparisons have been done in order to confirm the performance of the converter theoretically, simulation wise, and via experimentation. Table 4.2 shows the results of comparisons for open loop verification for operation mode one.

**Table 4.2:** Comparison of Selected Results Obtained from Operation Mode One

| Parameter | Theoretical | Simulation | Experiment |
|---|---|---|---|
| $V_o$ | 328 V | 99.4 % | 96.1 % |
| $V_{C1}$ | 280 V | 97.3 % | 85.7 % |
| $V_{C2}$ | 120 V | 103.9 % | 83.3 % |
| $V_{C3}$ | 160 V | 92.7 % | 87.5 % |
| $i_o$ | 0.328 V | 99.4 % | 96 % |
| $I_{L1}$ | 2.624 A | 99.1 % | 80.8 % |
| $I_{L2}$ | 4.373 A | 99.4 % | 96.7 % |

For the open loop operation in mode two, Table 4.3 shows the results obtained in each case.

**Table 4.3:** Comparison of Selected Results Obtained from Operation Mode Two

| Parameter | Theoretical | Simulation | Experiment |
|---|---|---|---|
| $V_o$ | 320 V | 99.5 % | 97.3 % |
| $V_{S3}$ | 0.8 V | 93.75 % | 91.25 % |
| $V_{S4}$ | 13.6 V | 99.56 % | 96.3 % |
| $i_b$ | 7.33 A | 96.86 % | 74.9 % |

For the open loop operation in mode three, Table 4.4 shows the results obtained in each case. There are some variations which stem from non-ideal components or equipment, electromagnetic interference or the presence of some undamped ringing in the waveforms. Such variations due are expected since the designed converter has no provisions to damp ringing and is produced with inherently non-ideal components.

**Table 4.4:** Comparison of Selected Results Obtained from Operation Mode Three

| Parameter | Theoretical | Simulation | Experiment |
|---|---|---|---|
| $V_o$ | 302.5 V | 99.87 % | 99.6 % |
| $V_{C1}$ | 280 V | 89.64 % | 86 % |
| $i_b$ | 6.62 A | 98.2 % | 93.8 % |

Comparisons of the simulation results for open loop and closed loop dynamic response are presented in Table 4.5. It can be observed that overshoot is reduced to zero at the selected reference voltages from 48 *V* and 61 *V* overshoot for output voltage of 250 *V* and 300 *V* respectively. For the settling time, the use of the controller for the 250 V output voltage delivered the 0.12 seconds (40 % reduction) settling time as against 0.2 seconds delivered without the controller. Similarly for the 300 V output voltage, the controller delivered the 0.15 (31.8 % reduction) seconds settling time as against 0.22 seconds delivered without the controller. These confirm the capability of the neural network controller to eliminate overshoot and reduce settling time and rise time of the proposed converter.

**Table 4.5:** Comparison between Open Loop and Closed Loop Simulation Results

| Testing | $V_{ref}$ | $V_1$ | $V_2$ | $d_1$ | $d_2$ | Overshoot | Settling time | $V_{out}$ |
|---|---|---|---|---|---|---|---|---|
| Open Loop | 250 V | 12 V | 24 V | 0.68 | 0.61 | 48 | 0.2 sec | 250 V |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Closed Loop | 250 V | 12 V | 24 V | 0.59 | 0.64 | 0 | 0.12 sec (40 %) | 250 V |
| Open Loop | 300 V | 12 V | 24 V | 0.7 | 0.68 | 61 | 0.22 sec | 300 V |
| Closed Loop | 300 V | 12 V | 24 V | 0.61 | 0.7 | 0 | 0.15 sec (31.8 %) | 300 V |

Table 4.6 shows the results of comparisons for open-loop and closed-loop dynamic response for experimental testing. For the settling time, the use of the controller for the 350 V output voltage delivered the 0.07 seconds (30 % reduction) settling time as against 0.1 seconds delivered without the controller. In similar fashion for the simulation results shown in Table 4.5, the experimental result in Table 4.6, confirm capability of the neural network controller to eliminate overshoot and reduce settling time and rise time of the proposed converter.

**Table 4.6:** Comparison between Open Loop and Closed Loop Experimental Results

| **Testing** | $V_{ref}$ | $V_1$ | $V_2$ | $d_1$ | $d_2$ | **Overshoot** | **Settling time** | $V_{out}$ |
|---|---|---|---|---|---|---|---|---|
| Open Loop | 350 V | 12 V | 24 V | 0.75 | 0.72 | 20 | 0.1 sec | 350 V |
| Closed Loop | 350 V | 12 V | 24 V | 0.62 | 0.74 | 0 | 0.07 sec (30 %) | 350 V |

### 4.5.1 Output Voltage Range of Proposed Three-Input Converter

It is necessary to identify the range of output voltage that is achievable by the proposed converter in its primary operation mode. This was carried firstly by identifying the lowest obtainable output voltage by operating the proposed converter with only one input

source at the lowest duty ratios, $d$ = 0.05. The lowest output voltage at 21.4 $V$ is measured when $V_1$ = 12 $V$ is the sole input source.

Figure 4.54 shows a plot of the measured output voltage against the duty ratio for an assumed PV input source at $V_1$ = 12 $V$, and 0.05 ≤ $d_1$ ≤. 0.75 with a 0.05 step increment. Similarly, at $V_2$ = 24 $V$, the output voltage range for that input source can be obtained. Figure 4.55 shows a plot of the measured output voltage against the duty ratio for an assumed FC input source at $V_2$ = 24 $V$, and 0 ≤ $d_2$ ≤ 0.75 with a 0.05 step increment.

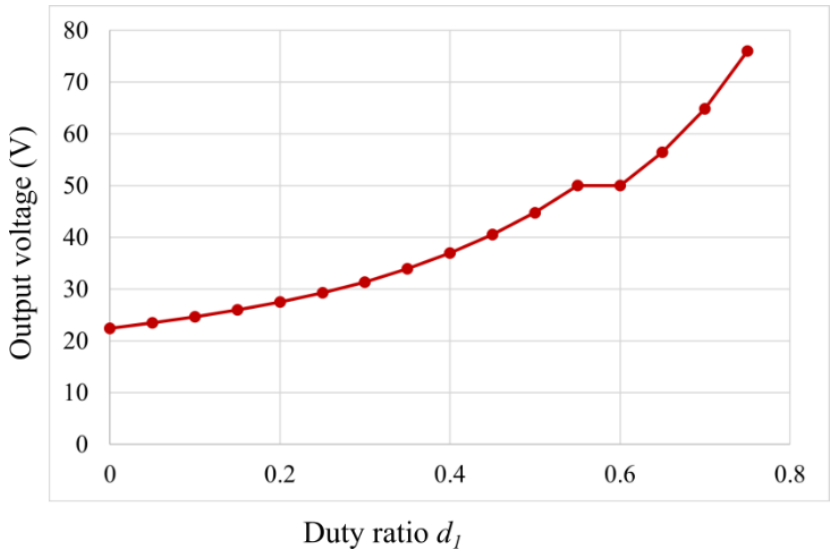


**Figure 4.54:** Plot of Measured Output Voltage against Duty Ratio $d_1$ for Single Input $V_1$

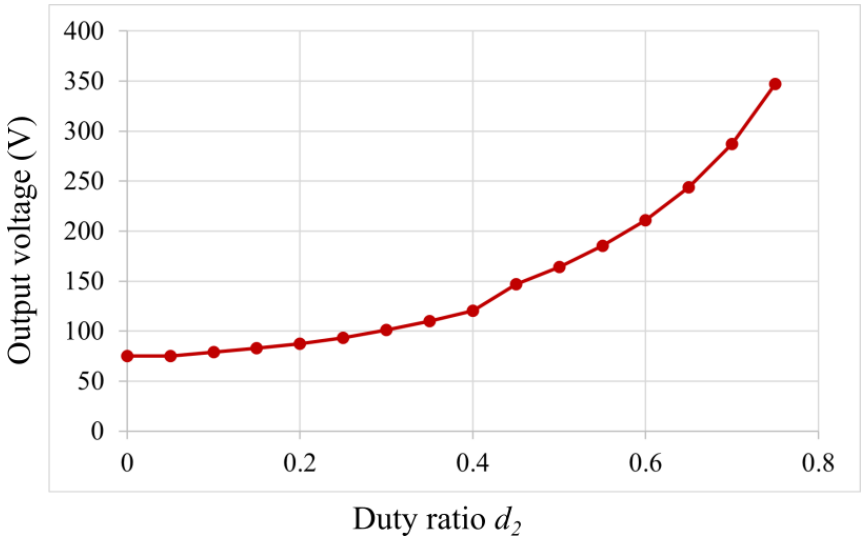


**Figure 4.55:** Plot of Measured Output Voltage against Duty Ratio $d_2$ for Single Input $V_2$

For the two input sources in the first operation mode, with $V_1$ =12 $V$, $V_2$ = 24 $V$, the duty ratio $d_1 = d_2 = d$, was incremented from 0.05 to 0.75. Figure 4.56 shows a plot of the measured output voltage against the duty ratio. The plotted output voltage ranges between 84 $V$ and 381 $V$. This indicates that an output voltage range 21.4 $V$ to 381 $V$ can be delivered by the proposed converter using single input, two input or three input sources.

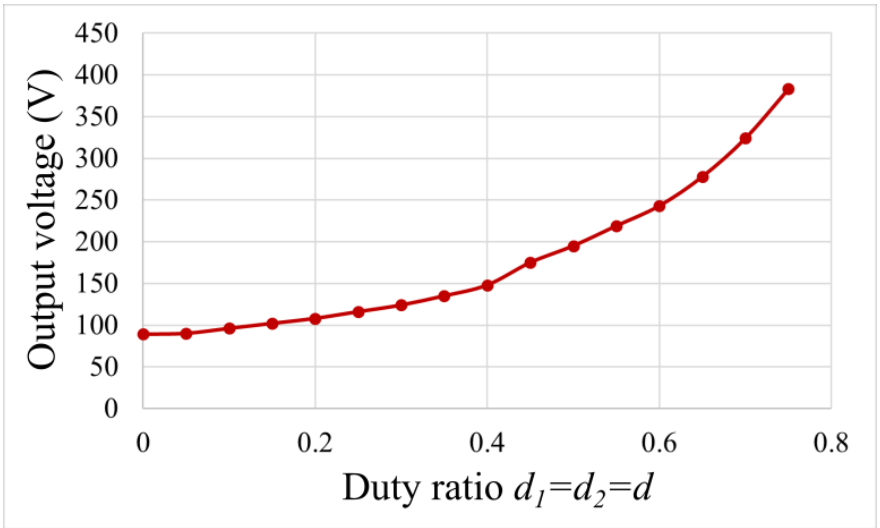


**Figure 4.56:** Plot of Measured Output Voltage against Duty Ratio $d_1 = d_2$ for Double Input Sources $V_1$ and $V_2$

## 4.6 Chapter Summary

In this chapter, the results of simulation and experimental validation of the proposed three-input converter have been presented. In addition, the steps taken in conducting these simulations and hardware integrations with the software have been described and justified. Results have been presented for the respective operation modes and some important characteristics of the proposed converter have been highlighted. The proposed ANN controller has been implemented and tested for all the operation modes, to demonstrate the dynamic response in different scenarios. Finally, the theoretical, simulation and experimental results have been compared and found to conform.

# CHAPTER 5

# CONCLUSION AND FUTURE WORK

## 5.1 Conclusion

The theoretical and practical enhancements to the battery integrated three input high gain DC-DC converter for RE applications have been presented in this thesis. The configuration developed combined the non-coupled inductor technique with the boost converter to attain a theoretical output voltage of 328 *V* during the first working mode. This stated output voltage can be achieved with input voltage level of 12 *V* and 24 *V* respectively for $V_1$ and $V_2$. The three working modes imply that that the battery can be charged, discharged or bypassed as the scenario arises. The theoretical output voltages of the second and third operation modes are 320 *V* and 302.5 *V* respectively. The analyses and modelling indicate that the input currents of the input voltage sources are dependent on the output current and the duty ratios of the specific supply switches. It also applies that the output voltage delivered separately by either of the non-coupled and boost side in the converter depend on the duty ratios of the dedicated power switch. Other than the power switch associated with the non-coupled inductor side, the voltage stress of the switches is marginally low.

The peculiar nature of RE sources as regards availability or irregular supply has been tackled by the energy management algorithm proposed for the BITIHGC. The algorithm makes it possible for BITIHGC to serve a load via single input, double input or three-input depending on the input power available, load power requirement and battery *SOC*. The six-neuron ANN voltage control that has been adopted, helped avoid the decoupling challenges posed by linearised controllers while regulating the output voltage in operation mode one.

The working modes of the proposed BITIHGC have been simulated. Also simulated, is the artificial neural network controller. The output voltage obtained in the respective operation modes during open loop simulation are in agreement with the theoretical values. The simulated output voltages are 326.1 *V*, 318.3 *V* and 302.1 *V* in the first, second and third operating mode respectively. The descending and ascending battery SOC profiles confirmed the discharging and charging as required during the second and third operation modes. During simulation, overshoots were non- existent when the ANN control was employed. In addition, for a 300 *V* output voltage, using the controller in the closed loop simulation, reduced the settling time by 31.8 % as compared to the open loop simulation without the controller.

The working modes and voltage controller of the proposed BITIHGC have been verified experimentally. The measured output voltages are 315 *V*, 311.5 *V* and 301.3 *V* in the first, second and third operating mode respectively. The results have shown that switches $S_1$, and $S_2$ determine the ports that deliver power to the load at any instant in the primary operation mode. Therefore, the amount of power provided from input voltage sources can be manipulated to obtain the required regulated output voltage by manipulating the duty ratios, $d_1$, $d_2$, utilizing the proposed NN control to manage the power to the load. Switches, $S_3$ and $S_4$ determine the battery charging and battery discharging modes. However, only the duty ratio, $d_4$ need be controlled to dictate either battery discharge to the load or the battery charging current depending on the existing load requirement. The ANN control implemented showed good voltage regulation in the close loop case for these experimental results. The success recorded during simulation was repeated during the experiment by the total elimination of overshoots. Compared to the open loop, the settling time was reduced by 30 %.

Finally, the developed BITIHGC finds applicability in hybrid RE systems that may wish to harness PV, FC and battery sources. The benefit of high voltage gain provided by the non-coupled inductor / boost technique could be extended to other applications, such as bidirectional converter in the hybrid electric vehicles and PV system.

## 5.2 Future Work

Future research on the non-coupled inductor may focus on mitigating losses associated with voltage stresses and current spikes during converter operation while maintaining the advantage of high voltage gain. Due to such limitations, designers currently have to trade-off on the desired characteristics of the MICs. Also worthy of investigation is the inclusion of a multiple bidirectional output ports in the three-input converter. The current regulation can be better by combining another type of non-linear control method with the ANN controller. Finally, extending the ANN control to a battery management system for the three-input converter would greatly improve the performance. Such work would require a consistent update of the battery SOC in the second and third operation mode, alongside updating the online learning algorithm of the ANN programme.

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Zhang, J., Wu, H., Huang, J., Xing, Y., & Ma, X. (2014). A novel multi-port bidirectional converter for interfacing distributed DC micro-grid. In *Proceedings of the IEEE International Symposium on Industrial Electronics* (pp. 2344–2348).

Zhang, N., Sutanto, D., & Muttaqi, K. M. (2016). A buck-boost converter based multi-input DC-DC/AC converter. In *Proceedings of the IEEE International Conference on Power System Technology* (pp. 1–6).

Zhang, Z., Thomsen, O. C., Andersen, M. A. E., & Nielsen, H. R. (2012). Dual-input isolated full-bridge boost DC-DC converter based on the distributed transformers. *IET Power Electronics, 5*(7), 1074–1083.

Zhang, Z., Thomsen, O. C., Andersen, M. A. E., & Nielsen, H. R. (2011). A novel dual-input isolated current-fed DC-DC converter for renewable energy system. In *Proceedings of the IEEE Applied Power Electronics Conference and Exposition* (pp. 1494–1501).

Zhang, Z., Thomsen, O. C., Andersen, M. A. E., & Nielsen, H. R. (2012). Dual-input isolated full-bridge boost DC-DC converter based on the distributed transformers. *IET Power Electronics, 5*(7), 1074–1083.

Zhao, R., & Kwasinski, A. (2009). Multiple-input single ended primary inductor converter (SEPIC) converter for distributed generation applications. In *Proceedings of the IEEE Energy Conversion Congress and Exposition* (pp. 1847–1854).

Zhao, R., & Kwasinski, A. (2012). Analysis of decentralized controller for multiple-input converters. In *Proceedings of the IEEE Applied Power Electronics Conference and Exposition* (pp. 1853–1860).

Zhu, B., Zeng, Q., Vilathgamuwa, D. M., Li, Y., & She, X. (2019). Non-isolated high-voltage gain dual-input DC/DC converter with a ZVT auxiliary circuit. *IET Power Electronics, 12*(4), 861–868.

Zhu, H., Zhang, D., Athab, H. S., Wu, B., & Gu, Y. (2015). PV isolated three-port converter and energy-balancing control method for PV-battery power supply applications. *IEEE Transactions on Industrial Electronics, 62*(6), 3595–3606.

Zolfi, P., Vahid, S., & El-Refaie, A. (2021). A novel three-port DC-DC converter for integration of PV and storage in zonal DC microgrids. In *Proceedings of the IEEE International Conference on Industrial Technology* (pp. 285–291).

# APPENDICES

**Appendix A:** Journal Publications

1. **Affam**, **A.,** Buswig, Y. M., Othman, A. K. B. H., Julai, N. Bin, & Qays, O. (2021) A review of multiple input DC-DC converter topologies linked with hybrid electric vehicles and renewable energy systems. *Renewable and Sustainable Energy Reviews*, *135* (July 2020), 110186, 1–23
2. **Affam, A.,** Buswig, Y. M. Y., Othman, A. H., Julai, N., & Albalawi, H. (2023). A battery integrated multiple input DC-DC boost converter. *Bulletin of Electrical Engineering and Informatics*, *12*(2), 677–688.
3. **Affam**, **A.,** Buswig, Y. M. Y., Othman, A. H., Salleh, S. F., Mohamed Basri, H., Julai, N., & Lias, K. (2024). Battery integrated three input high gain dc-dc converter for renewable energy sources. *International Journal of Power Electronics and Drive Systems* (Submitted and Under Review).

**Appendix B:** Comparison of Proposed Converter and Earliest Three-input Converter

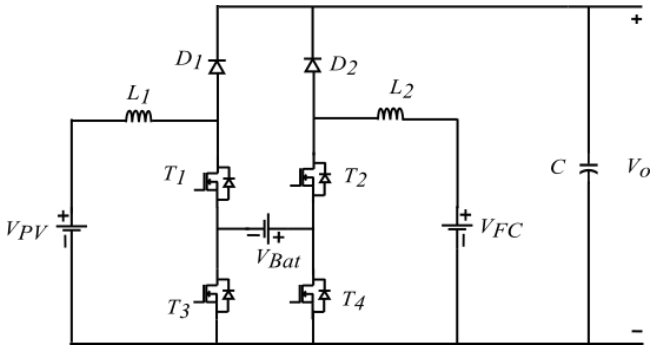



**Figure 1:** Circuit Diagram of Earliest Three Input Converter For PV/FC/ Battery (Feyzi et al., 2011)

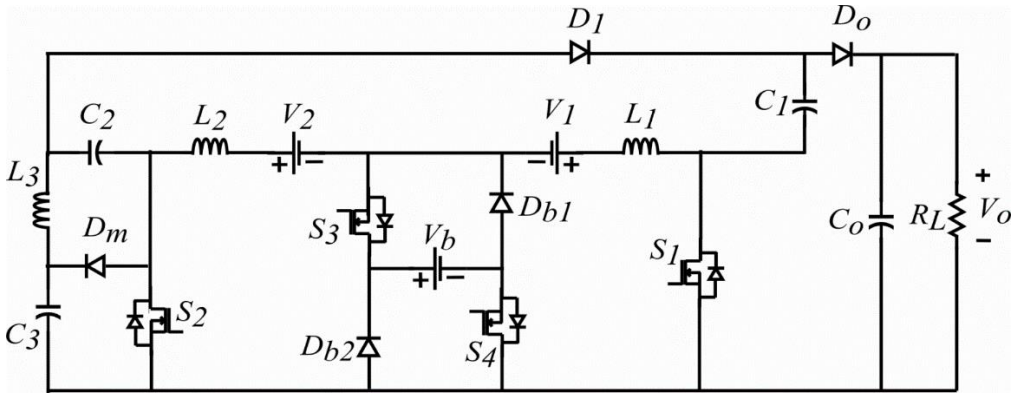



**Figure 2:** Circuit Diagram of Proposed Three Input Converter

**Appendix C:** Prototype

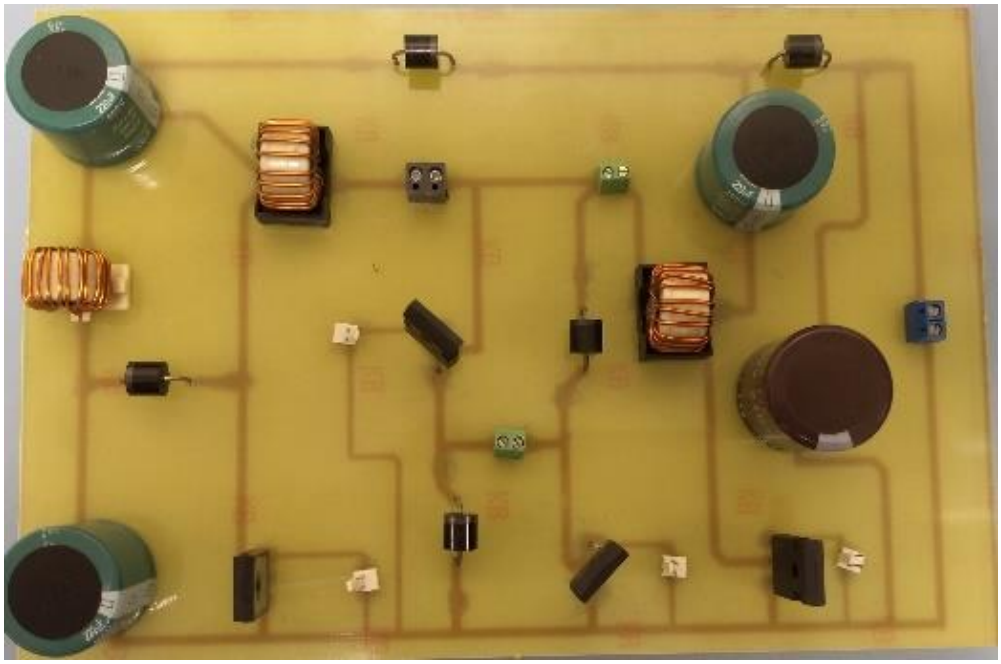


**Figure 3:** Prototype of BITIHGC

**Appendix D:** Source Code (C++ Language) of Switching pulse of Switches $S_1$& $S_2$ for Operation Mode One

```
#define S_FUNCTION_NAME swonetrial
#define S_FUNCTION_LEVEL 2

#include "simstruc.h"

#define U(element) (*uPtrs[element])  /* Pointer to Input Port0 */

static real_T A[1][1]={ { 1.0  } ,
                  };

/*====================*
 * S-function methods *
 *====================*/

/* Function: mdlInitializeSizes
================================================
 */
static void mdlInitializeSizes(SimStruct *S)
{
   ssSetNumSFcnParams(S, 0);  /* Number of expected parameters */
   if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
      return; /* Parameter mismatch will be reported by Simulink */
   }

   ssSetNumContStates(S, 0);
   ssSetNumDiscStates(S, 3);

   if (!ssSetNumInputPorts(S, 1)) return;
   ssSetInputPortWidth(S, 0, 1);
   ssSetInputPortDirectFeedThrough(S, 0, 1);

   if (!ssSetNumOutputPorts(S, 1)) return;
   ssSetOutputPortWidth(S, 0, 1);

   ssSetNumSampleTimes(S, 1);
   ssSetNumRWork(S, 0);
   ssSetNumIWork(S, 0);
   ssSetNumPWork(S, 0);
   ssSetNumModes(S, 0);
   ssSetNumNonsampledZCs(S, 0);

   /* Take care when specifying exception free code - see sfuntmpl_doc.c */
   ssSetOptions(S, SS_OPTION_EXCEPTION_FREE_CODE);
}
```

```
/* Function: mdlInitializeSampleTimes
=====================================
 *    Specifiy that we inherit our sample time from the driving block. */
static void mdlInitializeSampleTimes(SimStruct *S)
{
   ssSetSampleTime(S, 0, 0.00001);
   ssSetOffsetTime(S, 0, 0.0);
}

#define MDL_INITIALIZE_CONDITIONS
/* Function: mdlInitializeConditions
=====================================
 *    Initialize both discrete states to one. */
static void mdlInitializeConditions(SimStruct *S)
{
   real_T *x0 = ssGetRealDiscStates(S);
   int_T  lp;

   for (lp=0;lp<3;lp++) {
      *x0++=0.0;
   }
}

/* Function: mdlOutputs
=======================================================
 *      y = Cx + Du */
static void mdlOutputs(SimStruct *S, int_T tid)
{
   real_T           *y    = ssGetOutputPortRealSignal(S,0);
   real_T           *x    = ssGetRealDiscStates(S);
   InputRealPtrsType uPtrs = ssGetInputPortRealSignalPtrs(S,0);

   UNUSED_ARG(tid); /* not used in single tasking mode */

   if (x[0]<=((U(0)/1.5e4))-1e-6){
   y[0]=1;
   }
   else if (x[0]<=((1/1.5e4))){
   y[0]=0;
    }
   else if (x[0]<=((1/1.5e4)+(U(0)/1.5e4))){
   y[0]=1;
    }
   else {
   y[0]=1;
    }
```

```
}

#define MDL_UPDATE
/* Function: mdlUpdate
=================================================
 */
static void mdlUpdate(SimStruct *S, int_T tid)
{
   real_T           tempX[3] = {0.0, 0.0, 0.0};
   real_T           *x       = ssGetRealDiscStates(S);
   InputRealPtrsType uPtrs    = ssGetInputPortRealSignalPtrs(S,0);

   /* xdot=Ax+Bu */
   tempX[0]=(x[0]+0.000001);
   x[0]=tempX[0];
   if (x[0]>=(2/1.5e4-1e-6)){
   x[0]=0;
   }
}

/* Function: mdlTerminate
=================================================
 *    No termination needed, but we are required to have this routine.
 */
static void mdlTerminate(SimStruct *S)
{
   UNUSED_ARG(S); /* unused input argument */
}

#ifdef  MATLAB_MEX_FILE    /* Is this file being compiled as a MEX-file? */
#include "simulink.c"      /* MEX-file interface mechanism */
#else
#include "cg_sfun.h"       /* Code generation registration function */
#endif
```

**Appendix E:** Source Code (C++ Language) of Switching pulse of Switches $S_3$& $S_4$ for Operation Mode Two and Operation Mode 3

```
#define S_FUNCTION_NAME sw42
#define S_FUNCTION_LEVEL 2

#include "simstruc.h"

#define U(element) (*uPtrs[element])  /* Pointer to Input Port0 */

static real_T A[1][1]={ { 1.0  } ,
                  };


/*====================*
 * S-function methods *
 *====================*/

/* Function: mdlInitializeSizes
=============================================
 */
static void mdlInitializeSizes(SimStruct *S)
{
   ssSetNumSFcnParams(S, 0);  /* Number of expected parameters */
   if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
      return; /* Parameter mismatch will be reported by Simulink */
   }

   ssSetNumContStates(S, 0);
   ssSetNumDiscStates(S, 3);

   if (!ssSetNumInputPorts(S, 1)) return;
   ssSetInputPortWidth(S, 0, 1);
   ssSetInputPortDirectFeedThrough(S, 0, 1);

   if (!ssSetNumOutputPorts(S, 1)) return;
   ssSetOutputPortWidth(S, 0, 1);

   ssSetNumSampleTimes(S, 1);
   ssSetNumRWork(S, 0);
   ssSetNumIWork(S, 0);
   ssSetNumPWork(S, 0);
   ssSetNumModes(S, 0);
   ssSetNumNonsampledZCs(S, 0);

   /* Take care when specifying exception free code - see sfuntmpl_doc.c */
   ssSetOptions(S, SS_OPTION_EXCEPTION_FREE_CODE);
```

```
}

/* Function: mdlInitializeSampleTimes
=========================================
 *    Specifiy that we inherit our sample time from the driving block. */
static void mdlInitializeSampleTimes(SimStruct *S)
{
   ssSetSampleTime(S, 0, 0.00001);
   ssSetOffsetTime(S, 0, 0.0);
}


#define MDL_INITIALIZE_CONDITIONS
/* Function: mdlInitializeConditions
========================================
 *    Initialize both discrete states to one. */
static void mdlInitializeConditions(SimStruct *S)
{
   real_T *x0 = ssGetRealDiscStates(S);
   int_T  lp;

   for (lp=0;lp<3;lp++) {
      *x0++=0.0;
   }
}


/* Function: mdlOutputs
=======================================================
 *      y = Cx + Du */
static void mdlOutputs(SimStruct *S, int_T tid)
{
   real_T            *y    = ssGetOutputPortRealSignal(S,0);
   real_T            *x    = ssGetRealDiscStates(S);
   InputRealPtrsType uPtrs = ssGetInputPortRealSignalPtrs(S,0);

   UNUSED_ARG(tid); /* not used in single tasking mode */

   if (x[0]<=((U(0)/1.5e4)-1e-6)){
   y[0]=1;
   }
   else if (x[0]<=((1/1.5e4))){
   y[0]=1;
    }
   else if (x[0]<=((1/1.5e4)+(U(0)/1.5e4))){
   y[0]=1;
    }
   else {
```

```
   y[0]=0;
    }

}

#define MDL_UPDATE
/* Function: mdlUpdate
=================================================
 */
static void mdlUpdate(SimStruct *S, int_T tid)
{
   real_T           tempX[3] = {0.0, 0.0, 0.0};
   real_T           *x       = ssGetRealDiscStates(S);
   InputRealPtrsType uPtrs    = ssGetInputPortRealSignalPtrs(S,0);

   /* xdot=Ax+Bu */
   tempX[0]=(x[0]+0.000001);
   x[0]=tempX[0];
  if (x[0]>=(2/1.5e4)-1e-6){
   x[0]=0;
   }
}

/* Function: mdlTerminate
=================================================
 *    No termination needed, but we are required to have this routine.
 */
static void mdlTerminate(SimStruct *S)
{
   UNUSED_ARG(S); /* unused input argument */
}

#ifdef  MATLAB_MEX_FILE    /* Is this file being compiled as a MEX-file? */
#include "simulink.c"      /* MEX-file interface mechanism */
#else
#include "cg_sfun.h"       /* Code generation registration function */
#endif
```

**Appendix F:** Source Code (C++ Language) of Neural Network Control Algorithm

```
#define S_FUNCTION_NAME control20
#define S_FUNCTION_LEVEL 2
#include "simstruc.h"
#include "math.h"
#define U(element) (*uPtrs[element])  /* Pointer to Input Port0 */

//static real_T A[1][1]={ { -0.00000025  } ,
//static real_T A[1][1]={ {    0.000000051  } ,
static real_T A[1][1]={ {      0.00000000051  } ,                    };
static real_T B[1][1]={ { 1.0  } ,
                  };
/*====================*
 * S-function methods *
 *====================*/
static void mdlInitializeSizes(SimStruct *S)
{
   ssSetNumSFcnParams(S, 0);  /* Number of expected parameters */
   if (ssGetNumSFcnParams(S) != ssGetSFcnParamsCount(S)) {
      return; /* Parameter mismatch will be reported by Simulink */    }

   ssSetNumContStates(S, 0);
   ssSetNumDiscStates(S, 12);

   if (!ssSetNumInputPorts(S, 1)) return;
   ssSetInputPortWidth(S, 0, 5);
   ssSetInputPortDirectFeedThrough(S, 0, 1);

   if (!ssSetNumOutputPorts(S, 1)) return;
   ssSetOutputPortWidth(S, 0, 2);

   ssSetNumSampleTimes(S, 1);
   ssSetNumRWork(S, 0);
   ssSetNumIWork(S, 0);
   ssSetNumPWork(S, 0);
   ssSetNumModes(S, 0);
   ssSetNumNonsampledZCs(S, 0);

   ssSetOptions(S, SS_OPTION_EXCEPTION_FREE_CODE);
}

static void mdlInitializeSampleTimes(SimStruct *S)
{
   ssSetSampleTime(S, 0, 0.00001);
   ssSetOffsetTime(S, 0, 0.0);
}
```

```
#define MDL_INITIALIZE_CONDITIONS
static void mdlInitializeConditions(SimStruct *S)
{
   real_T *x0 = ssGetRealDiscStates(S);
   int_T  lp;

   for (lp=0;lp<1;lp++) {
   //  *x0++=1.45best;
   //  *x0++=1.0ori;
      *x0++=1.45;
   }
   for (lp=1;lp<2;lp++) {
   //  *x0++=1.0;
      *x0++=1.0;
   }
   for (lp=2;lp<3;lp++) {
//     *x0++=0.833ori;
//     *x0++=6;
       *x0++=0.00001;
   }
   for (lp=3;lp<4;lp++) {
    *x0++=0.00001;
//       *x0++=0.1;//ip=3 important to achieve value
   }
   for (lp=4;lp<5;lp++) {
//     *x0++=0.0000001-0.038-0.0472(final);
       *x0++=5;
   }
   for (lp=5;lp<6;lp++) {
   *x0++=0.0001;
 //      *x0++=0.0001;
   }
   for (lp=6;lp<12;lp++) {
      *x0++=0.0;
   }
}

static void mdlOutputs(SimStruct *S, int_T tid)
{
   real_T           *y    = ssGetOutputPortRealSignal(S,0);
   real_T           *x    = ssGetRealDiscStates(S);
   InputRealPtrsType uPtrs = ssGetInputPortRealSignalPtrs(S,0);

   UNUSED_ARG(tid); /* not used in single tasking mode */

    x[6]=x[0]*U(0)+x[3];
    x[7]=x[1]*U(1)+x[4];
    x[8]=x[2]*U(2)+x[5];
```

```
   x[9]=((2/(1+exp(-2*x[6])))-1);
   x[10]=((2/(1+exp(-2*x[7])))-1);
   x[11]=((2/(1+exp(-2*x[8])))-1);

   y[0]=x[9]+x[10]+x[11];
   y[1]= x[9]+ x[11];

}

#define MDL_UPDATE
static void mdlUpdate(SimStruct *S, int_T tid)
{
   real_T           tempX[6] = {0.0, 0.0, 0.0, 0.0, 0.0, 0.0};
   real_T           *x       = ssGetRealDiscStates(S);
   InputRealPtrsType uPtrs    = ssGetInputPortRealSignalPtrs(S,0);

   tempX[0]=x[0]-(U(3)*(1-(U(4)*U(4)))*x[0])*A[0][0];
   tempX[1]=x[1]-(U(3)*(1-(U(4)*U(4)))*x[1])*A[0][0];
   tempX[2]=x[2]-(U(3)*(1-(U(4)*U(4)))*x[2])*A[0][0];
   tempX[3]=x[3]-(U(3)*(1-(U(4)*U(4))))*A[0][0];
   tempX[4]=x[4]-(U(3)*(1-(U(4)*U(4))))*A[0][0];
   tempX[5]=x[5]-(U(3)*(1-(U(4)*U(4))))*A[0][0];
   x[0]=tempX[0];
   x[1]=tempX[1];
   x[2]=tempX[2];
   x[3]=tempX[3];
   x[4]=tempX[4];
   x[5]=tempX[5];
}

static void mdlTerminate(SimStruct *S)
{
   UNUSED_ARG(S); /* unused input argument */
}
#ifdef  MATLAB_MEX_FILE    /* Is this file being compiled as a MEX-file? */
#include "simulink.c"      /* MEX-file interface mechanism */
#else
#include "cg_sfun.h"       /* Code generation registration function */
#endif
```

**Appendix G:** dSPACE DS1104 Controller Board Overview

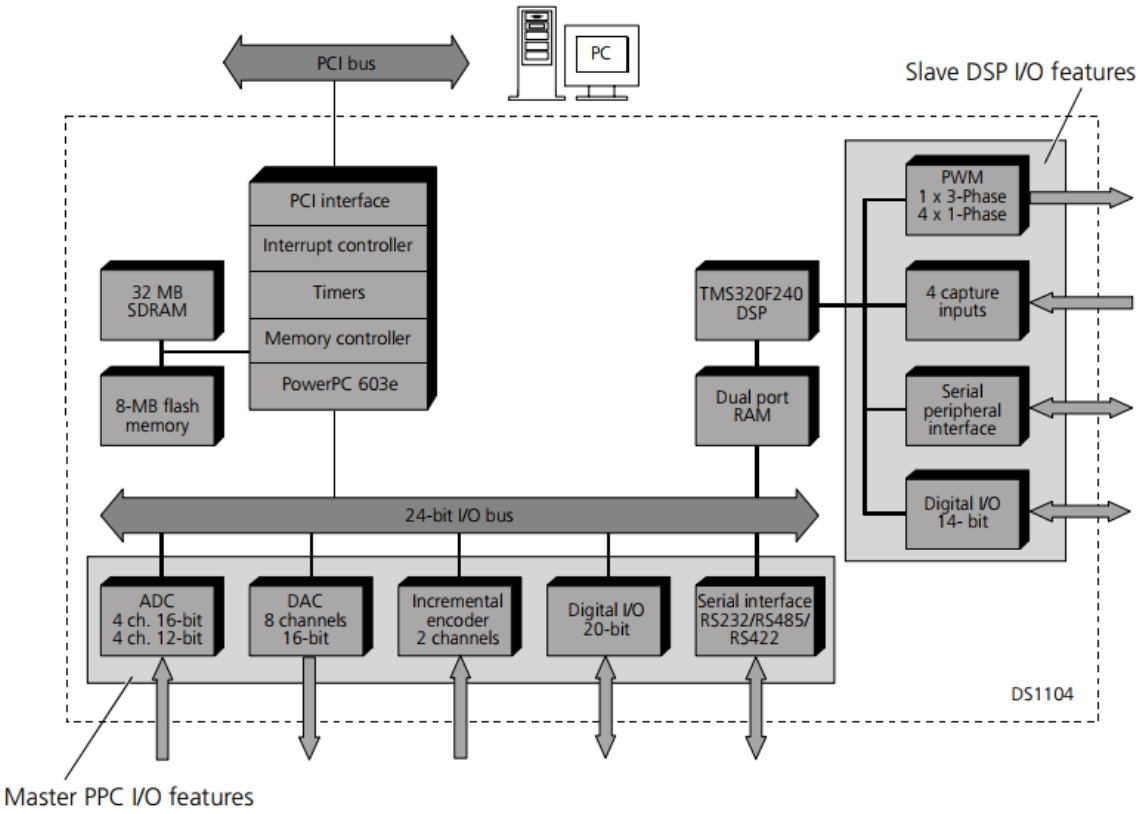



**Figure 4:** Architecture of dSPACE DS1104 Controller Board

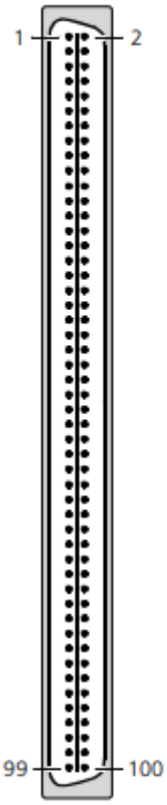
| I/O Connector (P1) | Pin | Sub-D Pin | Signal | Pin | Sub-D Pin | Signal |
|---|---|---|---|---|---|---|
|  | P1 1 | P1B 1 | GND | P1 2 | P1A 1 | GND |
| | P1 3 | P1B 34 | DCD (CTS) | P1 4 | P1A 34 | (RTS) |
| | P1 5 | P1B 18 | CTS (CTS) | P1 6 | P1A 18 | RTS (RTS) |
| | P1 7 | P1B 2 | DSR (RXD) | P1 8 | P1A 2 | DTR (TXD) |
| | P1 9 | P1B 35 | RXD (RXD) | P1 10 | P1A 35 | TXD (TXD) |
| | P1 11 | P1B 19 | SSOMI | P1 12 | P1A 19 | SCAP4 |
| | P1 13 | P1B 3 | SSIMO | P1 14 | P1A 3 | SCAP3 |
| | P1 15 | P1B 36 | SSTE | P1 16 | P1A 36 | SCAP2 |
| | P1 17 | P1B 20 | SSCLK | P1 18 | P1A 20 | SCAP1 |
| | P1 19 | P1B 4 | VCC (+5 V) | P1 20 | P1A 4 | VCC (+5 V) |
| | P1 21 | P1B 37 | ST3PWM | P1 22 | P1A 37 | SPWM6 |
| | P1 23 | P1B 21 | ST2PWM | P1 24 | P1A 21 | SPWM5 |
| | P1 25 | P1B 5 | ST1PWM | P1 26 | P1A 5 | SPWM4 |
| | P1 27 | P1B 38 | SPWM9 | P1 28 | P1A 38 | SPWM3 |
| | P1 29 | P1B 22 | SPWM8 | P1 30 | P1A 22 | SPWM2 |
| | P1 31 | P1B 6 | SPWM7 | P1 32 | P1A 6 | SPWM1 |
| | P1 33 | P1B 39 | GND | P1 34 | P1A 39 | GND |
| | P1 35 | P1B 23 | IDX(2) | P1 36 | P1A 23 | IDX(1) |
| | P1 37 | P1B 7 | IDX(2) | P1 38 | P1A 7 | IDX(1) |
| | P1 39 | P1B 40 | PHI90(2) | P1 40 | P1A 40 | PHI90(1) |
| | P1 41 | P1B 24 | PHI90(2) | P1 42 | P1A 24 | PHI90(1) |
| | P1 43 | P1B 8 | PHI0(2) | P1 44 | P1A 8 | PHI0(1) |
| | P1 45 | P1B 41 | PHI0(2) | P1 46 | P1A 41 | PHI0(1) |
| | P1 47 | P1B 25 | GND | P1 48 | P1A 25 | GND |
| | P1 49 | P1B 9 | IO19 | P1 50 | P1A 9 | IO18 |
| | P1 51 | P1B 42 | IO17 | P1 52 | P1A 42 | IO16 |
| | P1 53 | P1B 26 | IO15 | P1 54 | P1A 26 | IO14 |
| | P1 55 | P1B 10 | IO13 | P1 56 | P1A 10 | IO12 |
| | P1 57 | P1B 43 | IO11 | P1 58 | P1A 43 | IO10 |
| | P1 59 | P1B 27 | IO9 | P1 60 | P1A 27 | IO8 |
| | P1 61 | P1B 11 | IO7 | P1 62 | P1A 11 | IO6 |
| | P1 63 | P1B 44 | IO5 | P1 64 | P1A 44 | IO4 |
| | P1 65 | P1B 28 | IO3 | P1 66 | P1A 28 | IO2 |
| | P1 67 | P1B 12 | IO1 | P1 68 | P1A 12 | IO0 |
| | P1 69 | P1B 45 | GND | P1 70 | P1A 45 | GND |
| | P1 71 | P1B 29 | DACH8 | P1 72 | P1A 29 | DACH7 |
| | P1 73 | P1B 13 | GND | P1 74 | P1A 13 | GND |
| | P1 75 | P1B 46 | DACH6 | P1 76 | P1A 46 | DACH5 |
| | P1 77 | P1B 30 | GND | P1 78 | P1A 30 | GND |
| | P1 79 | P1B 14 | DACH4 | P1 80 | P1A 14 | DACH3 |
| | P1 81 | P1B 47 | GND | P1 82 | P1A 47 | GND |
| | P1 83 | P1B 31 | DACH2 | P1 84 | P1A 31 | DACH1 |
| | P1 85 | P1B 15 | GND | P1 86 | P1A 15 | GND |
| | P1 87 | P1B 48 | ADCH8 | P1 88 | P1A 48 | ADCH7 |
| | P1 89 | P1B 32 | GND | P1 90 | P1A 32 | GND |
| | P1 91 | P1B 16 | ADCH6 | P1 92 | P1A 16 | ADCH5 |
| | P1 93 | P1B 49 | GND | P1 94 | P1A 49 | GND |
| | P1 95 | P1B 33 | ADCH4 | P1 96 | P1A 33 | ADCH3 |
| | P1 97 | P1B 17 | GND | P1 98 | P1A 17 | GND |
| | P1 99 | P1B 50 | ADCH2 | P1 100 | P1A 50 | ADCH1 |



**Figure 5:** Pinout of I/O Connector for dSPACE DS 1104 Controller Board

**Appendix H:** Datasheets of Components

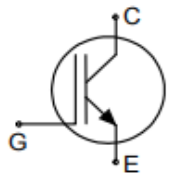
IGW25N120H3

High speed switching series third generation

## High speed IGBT in Trench and Fieldstop technology recommended in combination with SiC Diode IDH15S120

**Features:**

TRENCHSTOP™ technology offering
- best in class switching performance: less than 500µJ total switching losses achievable
- very low $V_{CEsat}$
- low EMI
- maximum junction temperature 175°C
- qualified according to JEDEC for target applications
- Pb-free lead plating; RoHS compliant
- complete product spectrum and PSpice Models: http://www.infineon.com/igbt/





**Applications:**

- solar inverters
- uninterruptible power supplies
- welding converters
- converters with high switching frequency

**Package pin definition:**

- Pin 1 - gate
- Pin 2 & backside - collector
- Pin 3 - emitter

Green

Halogen-Free

RoHS

**Key Performance and Package Parameters**

| Type | $V_{CE}$ | $I_C$ | $V_{CEsat}$, $T_{vj}$=25°C | $T_{vjmax}$ | Marking | Package |
|---|---|---|---|---|---|---|
| IGW25N120H3 | 1200V | 25A | 2.05V | 175°C | G25H1203 | PG-TO247-3 |

**Figure 6:** Data Sheet of IGBT

NIPPON CHEMI-CON

## CONDUCTIVE POLYMER ALUMINUM SOLID CAPACITORS

Radial Lead

Upgrade!

# NPCAP™-PSK Series

- Super low ESR, high ripple current capability
- Downsized from PSE series (φ6.3×8L to φ5×8L)
- Longer life (5,000 hours at 105℃)
- ESR after endurance is specified within the initial spec
- **RoHS Compliant**
- **Halogen Free**

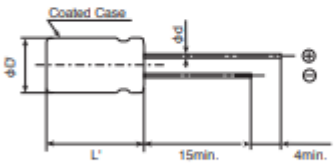

## ◆SPECIFICATIONS

| Items | Characteristics | |
|---|---|---|
| Category Temperature Range | −55 to +105℃ | |
| Rated Voltage Range | 2.5 to 6.3 Vdc | |
| Capacitance Tolerance | ±20% (M) | (at 20℃, 120Hz) |
| Surge Voltage | Rated voltage(V)×1.15 | (at 105℃) |
| Leakage Current*Note | 500μA max. | (at 20℃ after 2 minutes) |
| Dissipation Factor (tanδ) | 0.10 max. | (at 20℃, 120Hz) |
| Low Temperature Characteristics (Max.Impedance Ratio) | Z(−25℃)/Z(+20℃)≦1.15<br>Z(−55℃)/Z(+20℃)≦1.25 | (at 100kHz) |
| Endurance | The following specifications shall be satisfied when the capacitors are restored to 20℃ after the rated voltage is applied for 5,000 hours at 105℃. | |
| | Appearance | No significant damage |
| | Capacitance change | ≦±20% of the initial value |
| | D.F. (tanδ) | ≦The initial specified value |
| | ESR | ≦The initial specified value |
| | Leakage current | ≦The initial specified value |
| Bias Humidity Test | The following specifications shall be satisfied when the capacitors are restored to 20℃ after subjecting them to DC voltage at 60℃, 90 to 95% RH for 1,000 hours. | |
| | Appearance | No significant damage |
| | Capacitance change | ≦±20% of the initial value |
| | D.F. (tanδ) | ≦The initial specified value |
| | ESR | ≦The initial specified value |
| | Leakage current | ≦The initial specified value |
| Surge Voltage Test | The capacitors shall be subjected to 1,000 cycles each consisting of charge with the surge voltage specified at 105℃ for 30 seconds through a protective resistor(R=1kΩ) and discharge for 5 minutes 30 seconds. | |
| | Appearance | No significant damage |
| | Capacitance change | ≦±20% of the initial value |
| | D.F. (tanδ) | ≦The initial specified value |
| | ESR | ≦The initial specified value |
| | Leakage current | ≦The initial specified value |
| Failure Rate | 0.5% per 1,000 hours maximum (Confidence level 60% at 105℃) | |

*Note : If any doubt arises, measure the leakage current after the following voltage treatment.
Voltage treatment : DC rated voltage is applied to the capacitors for 120 minutes at 105℃.

## ◆DIMENSIONS [mm]

●Terminal Code : E




| Size code | E08 |
|---|---|
| φD | 5.0 |
| φd | 0.5(Note2) |
| F | 2.0 |
| φD' | φD+0.5max. |
| L' | L+1.0max. |

Note2 : 0.45 for rated voltage 2.5V

## ◆MARKING

EX) 2.5V560μF


**Figure 7:** Data Sheet of Output Capacitor

## ALUMINUM ELECTROLYTIC CAPACITORS

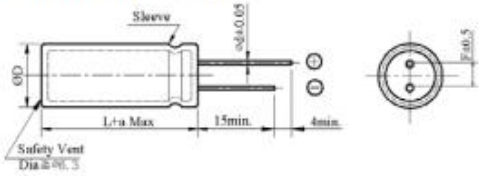
# PV Series

- **Downsize and high ripple current**
- **Load life 2,000 ~ 5,000 hours at 105℃**

◆ **SPECIFICATIONS**

| Item | Performance Characteristics |
|---|---|
| Category Temperature Range | -25 ~ +105℃ |
| Working Voltage Range | 200 ~ 450Vdc |
| Capacitance Range | 6.8 ~ 470 μF |
| Capacitance Tolerance | ±20% (at 25℃ and 120Hz) |
| Dissipation Factor (tanδ) (at 25℃ , 120Hz) | Rated Voltage (V): 200 / 250 / 350 / 400 / 420 / 450<br>tanδ(Max): 0.20 / 0.20 / 0.20 / 0.20 / 0.20 / 0.20<br>The above values should be increased by 0.02 for every additional 1000μF |
| Leakage Current | I=0.02CV or 3000 μA whichever is smaller<br>I : Leakage current (μA) C : Rated capacitance (μF) V : Rated voltage (V)<br>Impress the rated voltage for 2 minutes. |
| Endurance | The following requirements shall be satisfied when the capacitor are restored to 25℃ after the rated voltage applied for 2,000 to 5,000 hours at 105℃ .<br>Capacitance change ≦ ±20% of the initial value<br>Dissipation factor(tanδ) ≦ 200% of the specified value<br>Leakage current ≦ specified value<br>Size / Life time (hours): ΦD≦12.5Φ / 2,000; ΦD≧16 Φ / 5,000 |
| Shelf Life | The following requirements shall be satisfied when the capacitor are restored to 25℃ after exposing them for 1,000 hours at 105℃ without voltage applied.<br>Capacitance change ≦ ±20% of the initial value<br>Dissipation factor(tanδ) ≦ 200% of the specified value<br>Leakage current ≦ 200% of the specified value |
| Others | Conforms to JIS-C-5101-4 (1998), characteristic W. |

◆ **DIMENSIONS (mm)**




| ΦD | 10 | 12.5 L < 35 | 12.5 L ≥ 35 | 16 | 18 |
|---|---|---|---|---|---|
| ΦD | ΦD +0.5 Max | | | | ΦD +1.0 Max |
| Φd | 0.6 | 0.6 | 0.8 | 0.8 | 0.8 |
| F | 5.0 | 5.0 | | 7.5 | 7.5 |
| a | L + 1.5 Max | ≤ 35 L+1.5 Max<br>≥ 40 L+2.0 Max | | L + 2.0 Max | |

◆ **PART NUMBERING SYSTEM ( Example : 420V 68μF )**

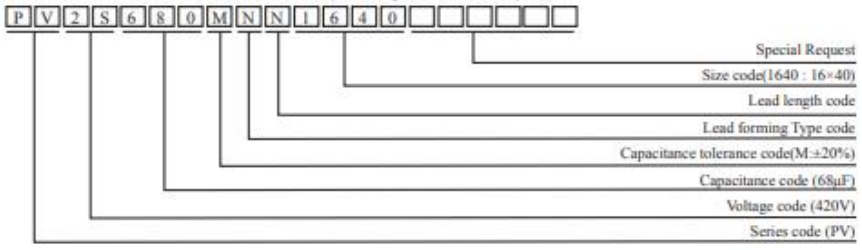
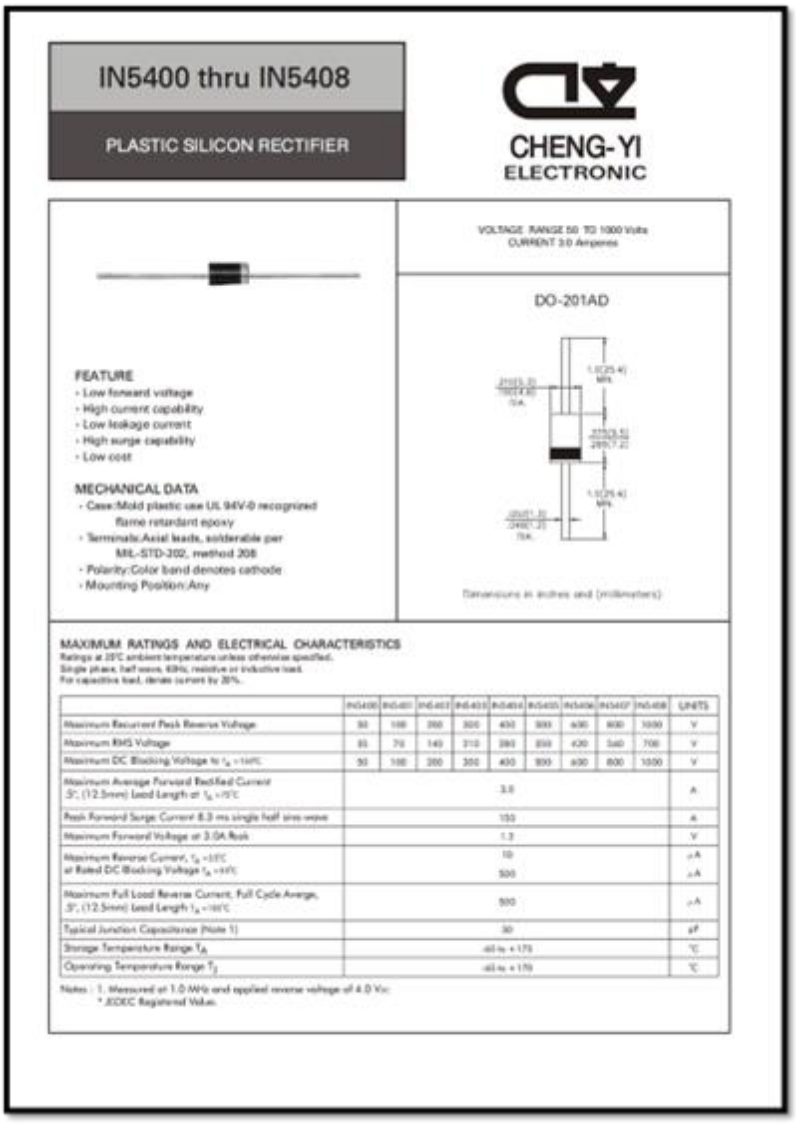



**Figure 8:** Data Sheet of Other Capacitors



IN5400 thru IN5408

PLASTIC SILICON RECTIFIER

CHENG-YI ELECTRONIC

VOLTAGE RANGE 50 TO 1000 Volts
CURRENT 3.0 Amperes

DO-201AD

FEATURE
- Low forward voltage
- High current capability
- Low leakage current
- High surge capability
- Low cost

MECHANICAL DATA
- Case:Mold plastic use UL 94V-0 recognized flame retardant epoxy
- Terminals:Axial leads, solderable per MIL-STD-202, method 208
- Polarity:Color band denotes cathode
- Mounting Position:Any

Dimensions in inches and (millimeters)

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.
Single phase, half wave, 60Hz, resistive or inductive load.
For capacitive load, derate current by 20%.

| | IN5400 | IN5401 | IN5402 | IN5403 | IN5404 | IN5405 | IN5406 | IN5407 | IN5408 | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| Maximum Recurrent Peak Reverse Voltage | 50 | 100 | 200 | 300 | 400 | 500 | 600 | 800 | 1000 | V |
| Maximum RMS Voltage | 35 | 70 | 140 | 210 | 280 | 350 | 420 | 560 | 700 | V |
| Maximum DC Blocking Voltage to $T_A$ =105°C | 50 | 100 | 200 | 300 | 400 | 500 | 600 | 800 | 1000 | V |
| Maximum Average Forward Rectified Current .5", (12.5mm) Lead Length at $T_A$ =75°C | 3.0 | | | | | | | | | A |
| Peak Forward Surge Current 8.3 ms single half sine-wave | 150 | | | | | | | | | A |
| Maximum Forward Voltage at 3.0A Peak | 1.2 | | | | | | | | | V |
| Maximum Reverse Current, $T_A$ =25°C<br>at Rated DC Blocking Voltage $T_A$ =100°C | 10<br>500 | | | | | | | | | μA<br>μA |
| Maximum Full Load Reverse Current, Full Cycle Average, .5", (12.5mm) Lead Length $T_A$ =105°C | 500 | | | | | | | | | μA |
| Typical Junction Capacitance (Note 1) | 30 | | | | | | | | | pF |
| Storage Temperature Range $T_A$ | -65 to +175 | | | | | | | | | °C |
| Operating Temperature Range $T_J$ | -65 to +150 | | | | | | | | | °C |

Notes : 1. Measured at 1.0 MHz and applied reverse voltage of 4.0 Vdc
* JEDEC Registered Value.

**Figure 9:** Data Sheet of Diode