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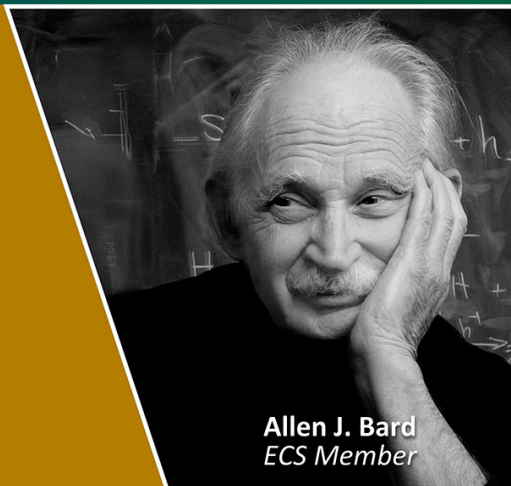


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A Linear 0.98 mV Low-Dropout Voltage Regulator in 0.18- μ m CMOS Technology

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Abstract. This paper presents a linear low-dropout (LDO) voltage regulator in 0.18- μ m CMOS technology. The proposed LDO consists of voltage reference, error amplifier, pass device, output capacitor and resistive feedback network. A symmetrical operational transconductance amplifier (OTA) is implemented as an error amplifier and a PMOS transistor is used as a pass device to produce low dropout voltage and low quiescent current. The proposed design is simulated using Spectre simulator in Cadence software to verify its performances. The simulation results indicated that the LDO regulator achieves a regulated output voltage of 1.5 V with the ranges of supply voltage from 1.7 V to 2.0 V. The LDO regulator has a dropout voltage of 19.3 mV under maximum load current of 1.1 mA. The proposed LDO regulator is suitable for power management system.

1. Introduction

Due to rising demand on the portable electronics devices, an on-chip power management system is required to stable the output voltage and prolonged battery life [1]. The power management system contains several components including linear voltage regulator, switching regulator and control logic. In general, a large voltage drop between the input and the output is required to ensure the linear voltage regulators function correctly [2]. A linear low dropout (LDO) voltage regulator is one of the linear voltage regulator circuit that can maintain the constant output voltages for any variation in the supply voltage or load currents. The LDO linear regulators are used to perform two functions; the first function is varying or regulates the output voltage required by the load. The second function is to keep the output voltage constant at the require value in spite of variation in the load current or supply voltage [3][4]. In fact, these functions are their main advantageous over the switching converters, where noise isolation and emissions are major system concerns.

The essential fundamental building block of power management unit is LDO regulator which is used in many portable batteries powered systems [5][6]. Since the constant and stable output voltage of LDO regulator independent of the load impedance, input voltage variation, temperature and time is required as the battery discharges. This characteristic leads to crucial stability improvement and noise reduction



for subsequent circuits. Due to the rapid growth of technology trend, designers are forced to design circuits operating at lower supply voltages. Thus, the LDO regulators are developed as they are ideal for giving multiple voltage levels and operate with a rather low dropout voltage. In addition, the LDO regulators also have capability of minimizing current consumption down to microamperes, which is important for current consumption of the sub-block in sleep mode. Another important characteristic of linear voltage regulator is their ability to suppress supply voltage noise, thus shielding the noise-sensitive blocks. Thus, PSRR is an important parameter of linear regulators. Besides that, the LDO linear voltage regulators are mostly used in IC design due to their performance, low cost and simplicity [5]. Therefore, the demand for the LDO regulators is increasing due to the higher demand of portable gadgets such as mobile phones, laptops, pagers as well as industrial and automotive applications [7].

Many types of LDO regulators have been proposed in the previous works to enhance the performance of the LDO regulators [1][2][5][13][17]. The most important parameters in designing the LDO regulator are the dropout voltage. Thus, the LDO voltage regulator has been designed by using bulk modulation technique that modulates the bulk voltage of the pass element to improve the dropout voltage of the LDO regulator [12]. The proposed LDO regulator has the dropout voltage of 200 mV. Besides that, the LDO voltage linear regulator based on a two-stage cascoded OTA as error amplifier is proposed in 0.13- μm CMOS technology has lower dropout voltage of 32 mV [16]. Based on the previously published works, the low dropout voltage can be achieved from 30 mV to 200 mV.

In this paper, a novel LDO voltage regulator is proposed using 0.18- μm CMOS technology. A symmetrical OTA as an error amplifier with a PMOS transistor as a pass element are employed to reduce the dropout voltage.

2. Circuit Design

The schematic design of the proposed low-dropout (LDO) voltage regulator is presented in **Figure 1**. All bulks of NMOS transistors are connected to ground and all bulks of PMOS are connected to supply. The circuit consists of a symmetrical operational transconductance amplifier (OTA), a voltage reference, a PMOS pass transistor, an external load capacitor with small value of equivalent series resistance (ESR), and a resistive feedback network. The voltage reference is used to bias the differential pair of M1 and M2 and the biasing transistor of M4 to stay in saturation region. Symmetrical OTA as an error amplifier in negative feedback condition detects an error signal when there is a difference between the feedback voltage and reference voltage. Transistors M3, M4, M5, M6, M7, M8, M9 and M10 form the simple current mirrors. Transistor M_{pass} as a pass device is used to drain current from the supply to the load. Output capacitor C_{out} and equivalent series resistance RESR are connected in the output node to provide stability for the circuit. Resistive feedback network consists of resistors R_{FB1} and R_{FB2} operating as a voltage divider to set the voltage for M2.

The proposed LDO regulator is designed based on the following parameters. The input voltage range is 1.7 V to 2.0 V, an input reference voltage is 1.2 V, an output voltage is 1.5 V and a biasing current is 100 nA.

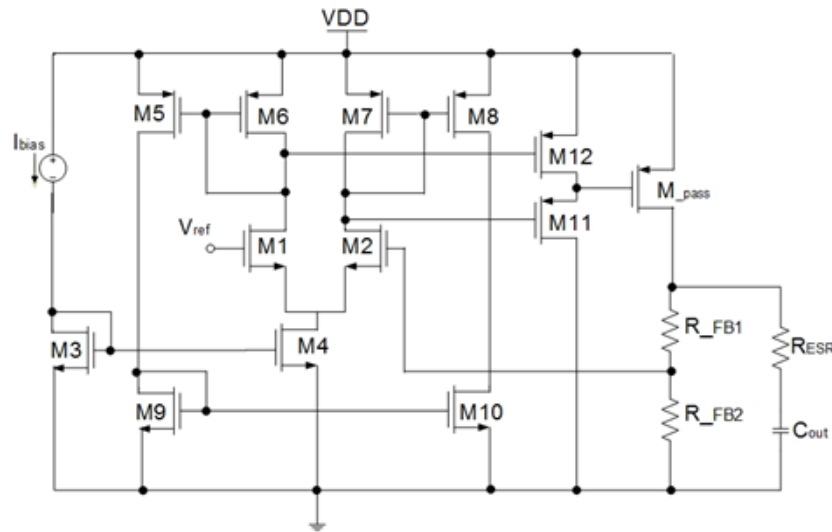


Figure 1. The proposed LDO voltage regulator schematic.

3. Simulation Results

Three types of analysis are performed to verify the LDO regulator performance includes DC analysis, transient analysis and AC analysis. The DC analysis focuses on steady state parameters of the LDO. Meanwhile, transient analysis computes the LDO's response as a function of time and AC analysis calculates the small-signal response of the LDO regulator.

The input-output voltage characteristics of the proposed LDO regulator is obtained by sweeping the DC input voltage supply from 0 V to 2 V as shown in **Figure 2**. The characteristic is obtained under maximum load current (I_{load}) conditions of 1.1 mA in order to verify the dropout voltage value. As observed from **Figure 2**, the output voltage of 1.5 V remains regulated for an input voltage range from 1.5 V to 2 V. The dropout voltage value was obtained at the beginning of the regulation region of VDO = 19.3 mV@ $V_{out} = 1.5$ V. There is no dropout voltage in the dropout region since the input voltage increases linearly with the output voltage. According to the result, it can be seen that the LDO regulator is in the regulation region when the output voltage level is high enough so that the LDO regulator can perform its two main functions such as keep the output voltage stable and deliver the required current to the load.

The line regulation is defined as the change at the output voltage in response to a change in the input voltage at a constant load current as express in equation (1).

$$Line\ regulation = \frac{\Delta V_{out}}{\Delta V_{in}} \quad (1)$$

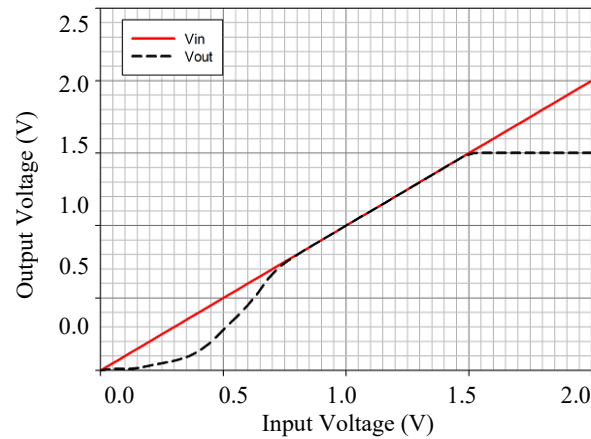


Figure 2. Input-output characteristics when the output voltage is $V_{out} = 1.5V$.

Figure 3 illustrates how the output voltage changes with the input voltage when the LDO operates in the linear region (regulating region). As can be seen, the line regulation of 1.67 mV/V is obtained for an output voltage of 1.5 V at a constant load current of 1.1 mA.

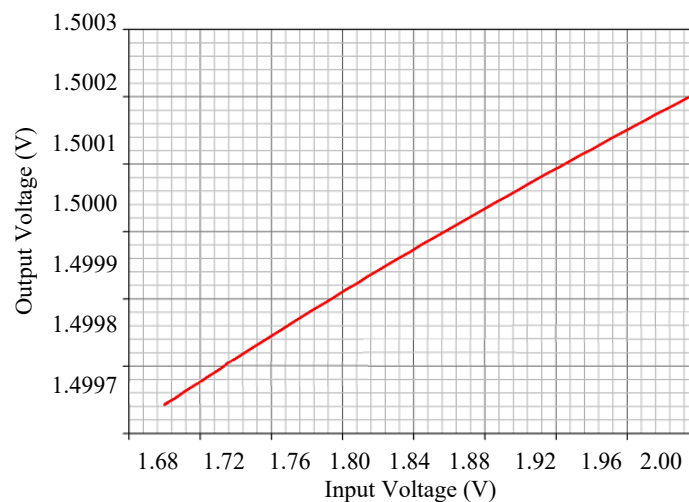


Figure 3. LDO regulator line regulation at $V_{out} = 1.5V$.

Figure 4 shows the load regulation when V_{in} is 1.7 V under maximum load current (I_{load}) conditions of 1.1 mA. The definition of load regulation is the change at the output voltage due to a change at the load current keeping the input voltage constant as given in equation (2).

$$Load\ regulation = \frac{\Delta V_{out}}{\Delta I_{out}} \quad (2)$$

Solving equation (2) with the values from the **Figure 4** results in a load regulation of 0.92 mV/mA for the output voltage of 1.5 V when the load current changes from 10 μA to 1.1 mA.

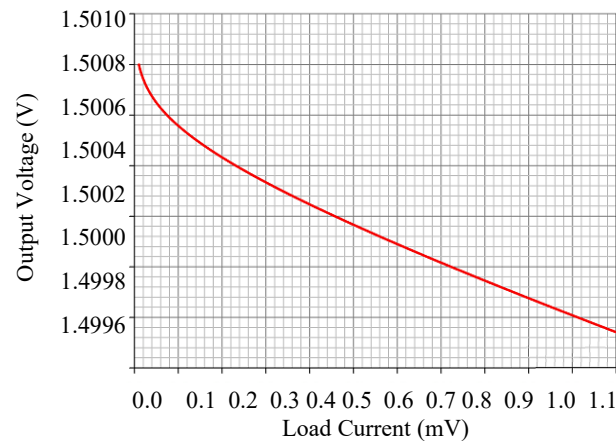


Figure 4. LDO regulator load regulation at $V_{out} = 1.5V$.

The other important parameters of LDO regulator are line and load transient responses. **Figure 5** shows the load transient response with frequency of 5 kHz. As observed, there is a small overshoot in the LDO output voltage which is in the range of millivolts. The overshoot is mainly caused by the equivalent series resistance (ESR) of the output capacitor. The larger of the current step and ESR, the larger the overshoot due to the capacitor is trying to source the current to the load.

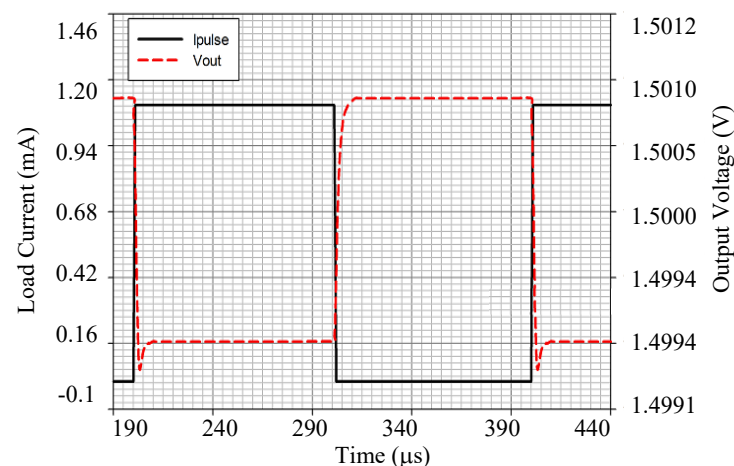


Figure 5. Load transient from 10 μA to 1.1 mA at 5 kHz.

Figure 6 depicts the line transient response for maximum load current 1.1 mA. As can be seen, it is clearly when the voltage rises, the response is fast, because the capacitor is charged by the current from the supply, but when the voltage drops, the output capacitor holds its value for quite a long time. This is because it is discharged only by a small amount of load current.

The LDO's stability parameter is measure by phase and gain margin. The phase margin needs to be at least 45° in order to has a stable system. **Figure 7** shows the bode plot of open loop gain and phase

over. The gain margin (GM) and the phase margin (PM) are plotted over frequency range from 1 Hz to 100 MHz. The GM is obtained when the phase is equal to 0° . The GM of the LDO regulator is -19.34 dB. Similarly, the PM margin is attained when the open-loop gain is equal to 0 dB. The LDO regulator has the phase margin of 69.5° . Therefore, the system is in stable condition.

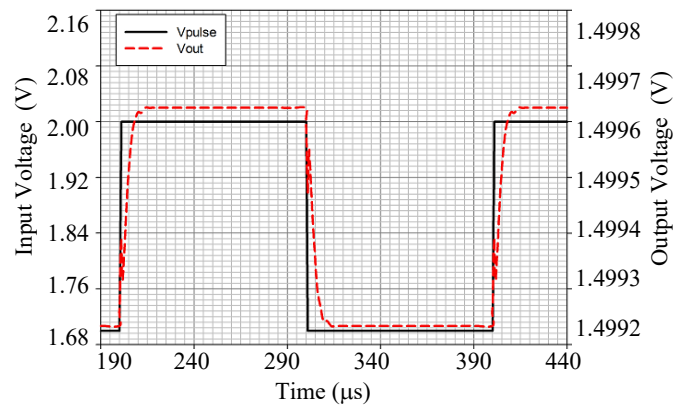


Figure 6. Line transient from 1.7 V to 2 V for load current of 1.1 mA.

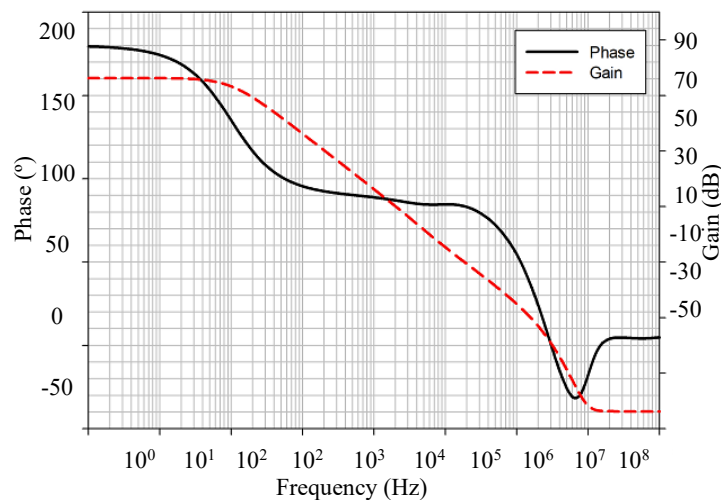


Figure 7. Bode plot of the proposed LOD.

The proposed LDO regulator is compared with other related works as shown in **Table I**. The LDO regulator with a double recycling folded cascode as an error amplifier is proposed in [13] and [17] produces the dropout voltage of 200 mV. The proposed LDO regulator in [16] which implements a main error amplifier and a bulk error amplifier with the bulk modulation technique provides the dropout voltage of 200 mV. The proposed LDO voltage regulator based on a two-stage cascoded OTA as an error amplifier with body driven technique in [16] gives same dropout voltage of 200 mV. In [14], the proposed LDO achieves low dropout voltage of 32 mV with a constant input voltage at 5 V. The proposed LDO in this work which implements a symmetrical OTA gives the lowest dropout voltage of 19.3 mV as compared to the others LDO regulators. In addition, the LDO achieves better line regulation as compared to the others LDO regulators. Moreover, the proposed LDO obtains the line regulation of 1.67 mV/V makes it as a useful choice in battery-powered portable applications, where the input voltage

is changing due to the battery discharging. Besides that, the proposed design has higher power supply rejection (PSR) of -54.92 dB when compared to the proposed LDO regulator in [12]. Based on Table I, the proposed LDO voltage regulator in this work indicate that the LDO is very promising to be implemented in power management for system on chip (SoC) applications.

4. Conclusion

A linear low-dropout (LDO) voltage regulator in 0.18- μm CMOS technology is successfully designed and simulated. A low dropout voltage and low quiescent current is achieved by using a symmetrical operational transconductance amplifier (OTA) and a PMOS transistor as an error amplifier and a pass device, respectively. The simulation results indicated that the LDO regulator achieves a regulated output voltage of 1.5 V with the ranges of supply voltage from 1.7 V to 2.0 V. The LDO regulator has a dropout voltage of 19.3 mV under maximum load current of 1.1 mA. The proposed LDO regulator is suitable for power management system.

Table 1. Comparison with previously published LDO voltage regulators.

Reference	[12]	[13]	[14]	[15]	[16]	[17]	[18]	This work
Year	2015	2017	2018	2018	2018	2019	2019	2020
CMOS Technology (μm)	0.18	0.13	0.13	0.18	0.18	0.18	0.18	0.18
Supply voltage (V)	1.45-2.0	1.2	5	1.8	2.0-3.3	1.2-1.8	1.8-2.6	1.7-2.0
Output voltage (V)	1.4	1	4.5	0.5	1.8	1.2-1.8	1.6	1.5
Dropout voltage (mV)	200	200	32.1	200	200	200	200	19.3
Load current (mA)	0-100	5	0.265	50	-	100	50	1.1
Line regulation (mA/V)	7.27	-	-	71.25	15.38	-	15.7	1.67
Load regulation (mV/mA)	0.016	0.015	-	-0.438	0.8	-	-	0.92
PSR at 1 kHz (dB)	-49.26	-	-	-	-	-	-	-54.92

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