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The analysis of soft error in static random access memory and mitigation by using transmission gate

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ABSTRACT

As the progress of technology continues in accordance to Moore's law, the density and downsizing of circuitry presents a significant vulnerability to the effects of soft errors. This study proposed a novel method to mitigate soft errors by increasing the robustness of complementary metal oxide semiconductor (CMOS) technology against soft errors via the use of transmission gates within the memory nodes of static random access memory (SRAM) which functioned as a low pass filter that disallowed the occurrence of data corruption. The proposed SRAM was tested against parameter variation of supply voltage and temperature. The critical charge was observed to increase with supply voltage increase, with the opposite being true of the increase in temperature. The increase in critical charge of up to 88.63% was achieved with regards to parameter variation for the transmission gate SRAM in comparison to the 6T SRAM.

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1. INTRODUCTION

The phenomenon of single event upsets cause digital integrated circuit (IC) technologies are at the risk of malfunctions. As the voltages, capacitances at the node, as well circuit dimensions reduce, their critical charges decrease with them, causing sub-micron technologies to become more easily affected by soft errors. Single event upsets are defined as errors caused by radiation when particles ionize the circuit nodes as they pass [1]. Single event upsets are attributed to two categories of radiation interactions, that being direct and indirect ionization [2]. A transient charge can be generated from the instance of a single event upset, wherein a circuit node is traversed by a particle. During a particle impact, the trajectory through which the particle travels induces alongside it a dense collection of electron-hole pairs.

Transistors in an inactive state are especially vulnerable in complementary metal oxide semiconductor (CMOS) circuits as particle strikes can cause changes in logic due to the alteration of the voltage at the node [3], [4]. The current pulse produced from the particle strike can induce a charge that, in the event that it exceeds the critical charge (Q_{crit}), which is the least amount of charge absorbed by the node needed to change the circuit state, causes a single event transient to form at the node. It thus stands to reason that a higher critical charge would be desirable in order to increase the soft error robustness, as critical charge has a direct impact on the severity of soft errors [5]. An issue with soft errors is that the system may not display weaknesses in hardware reliability following the occurrence of a soft error, as the issue is transient in nature and does not result in permanent hardware malfunctions.

Sensitive device nodes that are visited upon by ionised particles are subject to the process of soft error occurrence. A concentration of electron hole pairs will be disseminated along the trajectory of the

charged particle. In the case that this trajectory crosses the depletion region of a transistor node, the electric field will then collect the electron hole pairs [6]. The imbalanced distribution of charge causes a distortion along the particle path, leading to drift charge collection, followed by diffusion concluding the charge collection to completion. The distance from the junction is inversely proportional to the likelihood of the event transpiring. Data may become corrupted in the event that sufficient charge is collected. The critical charge refers to the minimum charge require to induce this event, hence correlating to the occurrence of soft errors.

The double exponential model for the transient current waveform with the collection charge can be calculated as (1) [7], [8]:

$$I(t) = \frac{Q_{total}}{\tau_f - \tau_r}(e^{-t/\tau_f} - e^{-t/\tau_r}) \quad (1)$$

The total charge is the charge collected from the instance of the particle strike, and the model has a rising time of τ_r and falling time of τ_f. The total charge produced from the single event upset is denoted by Q_{total}, with the rise and fall times selected as 50 ps and 164 ps respectively [9].

Static random access memory (SRAM) in its infancy, with its increased operating voltage and the use of its inverter loop for memory storage, presented a higher resistance against soft errors in comparison to dynamic random-access memory (DRAM). The node capacitance of the SRAM cell and the size of the transistor are the major factors that directly impact the critical charge. Generally, larger transistors are more resistant to soft errors by virtue of the higher switching threshold requiring a larger collection charge to cause data corruption. Downscaling efforts bring with it a notable reduction in capacitance and area, as well as a lower operating voltage to in the attempt to improve power minimization [10]. The effects of cell and pull up ratio also play a part in the design considerations against SRAM, as these ratios have a direct affect on the stability of the cell, which in turn determines the vulnerability of the given SRAM against single event effects [11].

The reductions in operating voltage and node capacitance with progression of SRAM generations. Each generation came with it an increase in SER which plateaus as feature sizes approach submicron levels [12]. The increase in scaling is accompanied with denser circuitry, leading to an exponential increase in SER with no predicted upper limit. Soft error occurrences are also exacerbated by the increase in SRAM operating frequencies, especially during read operations which have a relatively lower critical charge.

This study proposes a method to mitigate soft errors by increasing the robustness of CMOS technology against soft errors via the use of transmission gates within the memory nodes of SRAM. The mitigative method is based on that proposed by [13], [14]. In this case, the method was used in the memory nodes of a 6 transistor SRAM and the resulting critical charge was compared to that of a conventional 6 transistor SRAM of technology node 180 nm. The transmission gates function as a low pass filter that disallows the occurrence of data corruption as a result of the current pulse produced from a particle strike. Filters used to block transients have been employed in sensitive circuitry and function as low-pass filters. The use of pass transistors as filters have been investigated, wherein the suppressive quality of logic gates are used to attenuate transient input pulses [15]. The sizing of the transmission gates reflects that of the transmitters used in the SRAM cell, and is key that they are sized appropriately in order to effectively filter out transients. If the transistors of the transmission gate have a smaller size than the transistors used in the SRAM cell, it will not be able to exhibit a strong enough filtering effect to eliminate the transients [16]. The transmission gate method applies a reduced gate-source voltage to the n-channel metal oxide semiconductor (NMOS) pass transistor, and reduced source-gate voltage to the p-channel metal oxide semiconductor (PMOS) transistor, causing the increased resistance of the transmission gate to produce a strong filtering effect.

2. METHOD

The transient current induced from the particle strike is modelled as a double exponential current was illustrated as a trapezoidal shape as illustrated in Figure 1. The model has a fast rising time τ_{rise} and a slow falling time τ_{fall}. The rise and fall times for current pulse is 50 ps and 164 ps respectively [17]. The 6T-SRAM consists of six transistors, which make up two access transistors and an inverter loop. This current model will be injected into the memory node Q and QB of the SRAM. The aforementioned nodes maintain complementary bits of memory and can have this memory overwritten if the NMOS or PMOS experience a particle strike [18]. The Figure 2 shows the transmission gate and Figure 3 shows the SRAM with the transmission gate amended to the inverter node.

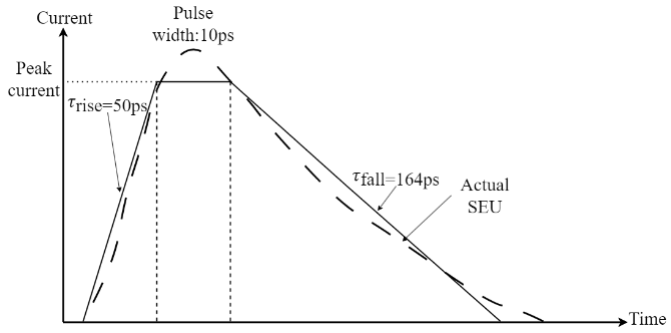


Figure 1. Analytical model of double exponential transient current

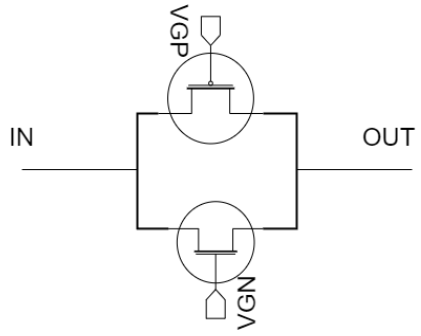


Figure 2. Transmission gate as transient filter

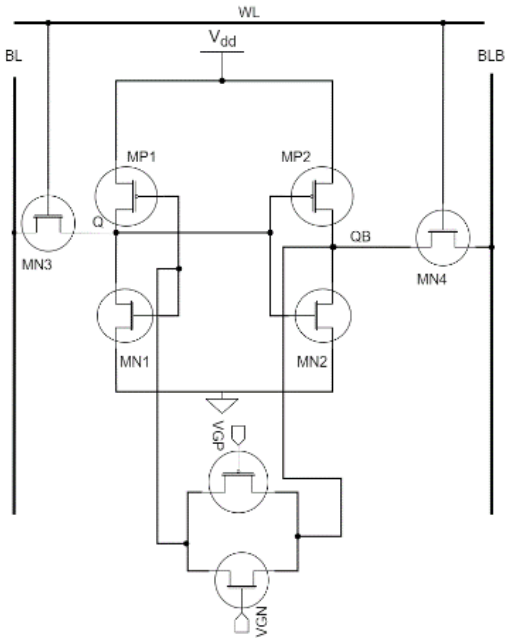


Figure 3. 6 TSRAM with transmission gate filter

The width/length (W/L) sizing for the access transistors are set at 450 nm/180 nm. For the storage inverter, the PMOS transistors MP1 and MP2 are sized at 220 nm/180 nm. The NMOS transistors MN1 and MN2 are sized at 720 nm/180 nm. The W/L must be sized so that during read operation, the cell must hold the stored state against the precharged bit-line. The cell ratio (CR) is the ratio of the driver against the access transistor, while the pull-up ratio (PR) is the ratio of load to access transistor [19]. The sizing was decided upon after testing various dimensions to achieve optimal robustness and area constraints as well as reference to existing literature [20].

$$CR = \frac{(W_{MN1}/L_{MN1})}{(W_{MN3}/L_{MN3})} = \frac{(W_{MN2}/L_{MN2})}{(W_{MN4}/L_{MN4})} \quad (2)$$

$$PR = \frac{(W_{MP1}/L_{MP1})}{(W_{MN3}/L_{MN3})} = \frac{(W_{MP2}/L_{MP2})}{(W_{MN4}/L_{MN4})} \quad (3)$$

The use of the transmission gate filter is based on the design proposed wherein a transmission gate is used to oppose the transient current produced by a single event upset [13]. The PMOS and NMOS transistors for the transmission gate are proposed to be set at 220 nm/180 nm and 720 nm/180 nm respectively. The transmission gates were sized as such in order to be able to capture the transient and to not obstruct the ability of the SRAM to store and overwrite data. The sizing also serves to better capture the transient current. The gate voltages V_{GN} and V_{GP} for the transmission gate NMOS and PMOS transistors are set at 0.71 V and 0.52 V respectively. This is to achieve an increased resistance from the transistors for a significant filtering effect to block transient signals. The length is also selected to slow the speed of the transistor which also serves to increase the transistor resistance. This is especially important when factors

come into play to reduce the robustness of systems against soft errors, such as operations in high temperatures or low voltage, with accompanying low node capacitance.

In read operations, the word line will engage and activate the access transistors, allowing the bit lines BL and BLB to access the inverter loop. The bitlines are precharged to V_{DD}, and in the case of Q holding the bit "0" and QB holding the bit "1", the transistor MN1 will turn on and discharge the BL to ground, allowing the bitline to hold the corresponding data "0". On the other hand, QB holding the data "1" will cause the transistor MP2 to turn on which will allow BLB to hold the data "1" at output. For the write operation, the bitlines will drive and overwrite the values in the inverter loops. To write a "0" into node Q, BL will be low and BLB will be driven high, causing the transistors MP1 to be turned off and MN1 to be activated. Q will be driven to ground, resulting in a "0" state. MP2 will be turned on, connecting QB to V_{DD} allowing it to hold a logic state "1".

The current pulse would be injected into the node Q and QB through the parametric variation function and increased in amplitude until the data was successfully flipped. As illustrated in Figures 4 and 5, the voltage level of the data is affected by the amplitude of the current pulse inserted. In Figures 4 and 5, at point (i), the current pulse is not significant enough to affect the stored bit. Point (ii) shows the current pulse is able to exceed 20% of the total voltage without causing a flip in the data. The point (iii) shows that the current pulse is able to flip the state from "0" to "1" in (a) and "1" to "0" in (b).

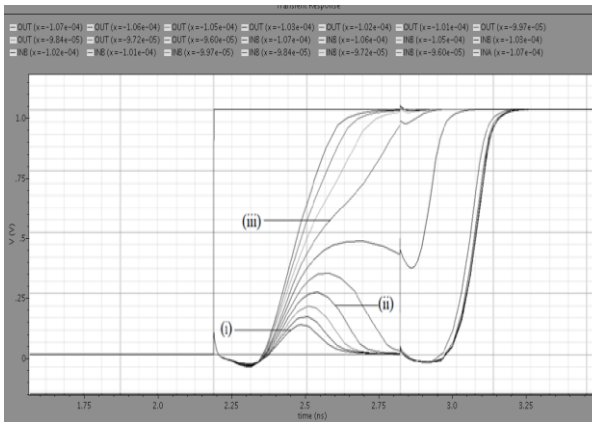


Figure 4. Injection of current pulse for 0-1

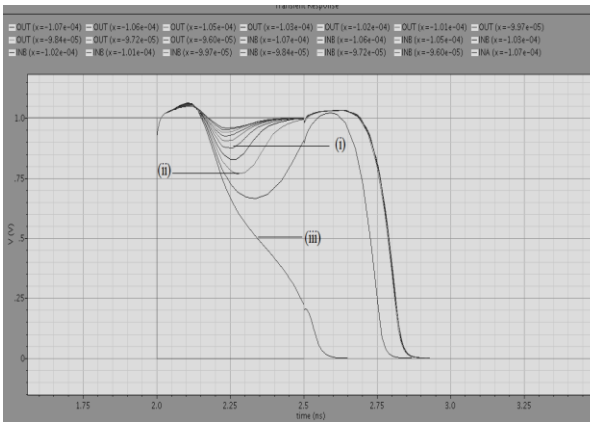


Figure 5. Injection of current pulse from 1-0

The initial state of "0" and "1" are set for node Q and QB respectively, with the supply voltage and temperature amended for each measurement. The voltage points are set from 0.7 V to 1.5 V with step intervals of 0.1 V set to temperature of 27 ºC. The temperature variations will be done with the supply voltage set to 1 V and with set points at -50 ºC, 0 ºC, 27 ºC, 125 ºC, and 200 ºC. In order to evaluate the effectiveness of the transmission gate at filtering the current pulse, the critical pulse of the nodes Q and QB was recorded with the nodes being connected to the respective nodes. The simulation was performed in Cadence Virtuoso with a technology node of 180 nm.

3. RESULTS AND DISCUSSION

3.1. 6T SRAM read state

The critical charge of the conventional 6T SRAM for the read operation was obtained. Figure 6 shows the critical charge against voltage variation (Figure 6(a)) and temperature (Figure 6(b)). As the layout of the SRAM cell has a symmetrical layout, the critical charge of nodes Q and QB are the same at the data states "0" and "1". The critical charge to change the data states of 0-1 and 1-0 for nodes Q and QB for the voltage ranges of 0.7 V to 1.5 V and temperature range of -50 ºC to 200 ºC. The supply voltage increase, shown in Figure 6(a), is followed by an increase in the driving current and corresponding node capacitance, thus the critical charge as well. This brings with it an added robustness to the cell as it becomes more difficult for the stored data to be overwritten. The critical charge for 0-1 increases by 357%, and for 123.78% for 1-0 as the voltage increases. The nodes for Q and QB for state transition 1-0 has a much lower critical charge in comparison, due to the smaller PMOS sizing to accommodate the need for a weak pull up power in order to write new data into the inverters. Figure 6(b) shows the critical charge for temperature variation from -50 ºC to 200 ºC. The temperature increase reduces the carrier mobility, but to a lesser extent compared to the

voltage supply variation [21]. As observed previously with Figure 6(a), the critical charge for 1-0 is lower than that of 0-1. As the temperature is increased, the critical charge decreases by 38% for 0-1 and 9% for 1-0.

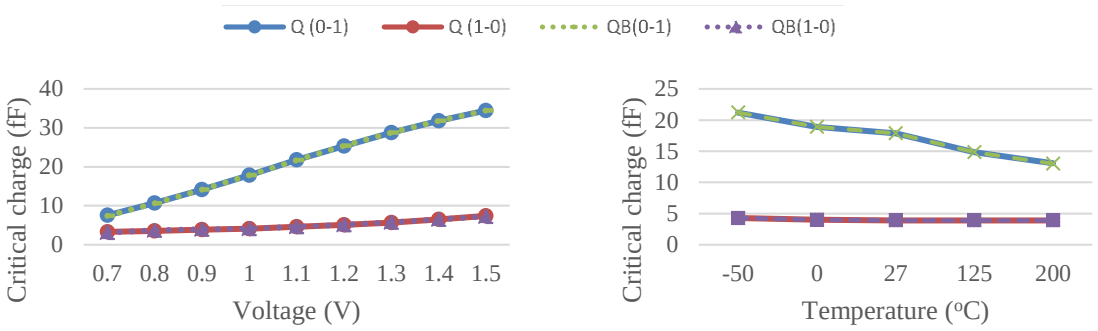


Figure 6. Graph of critical charge (fF) of 6T SRAM in read state against; (a) voltage (V) and (b) temperature (ºC)

3.2. 6T SRAM hold state

Figures 7(a) and (b) show the critical charge for the hold state when instated with parametric variation of voltage supply and temperature respectively. The critical charge follows similar trends to the read state in response to the voltage and temperature albeit to a reduced capacity due to the read state being relatively more susceptible to stored data being overwritten as the inverters are connected to precharged bitlines. As the voltage supply is increased, the critical charge increases as a response. As a result, the nodes Q and QB for 0-1 increase by 404% and by 184% for 1-0. For the temperature response, the critical charge decreases as the temperature increases. As the temperature is raised from -50 ºC to 200 ºC, the critical charge for the nodes Q and QB decreases by 34.26% and 5.81% for 0-1 and 1-0 respectively. From the read to the hold, the critical charge of the 6T SRAM at 1.5 V increases by 16.17% and 54% for 0-1 and 1-0 respectively. At 0.7 V, the increase is 5.24% and 21.31% respectively for 0-1 and 1-0.

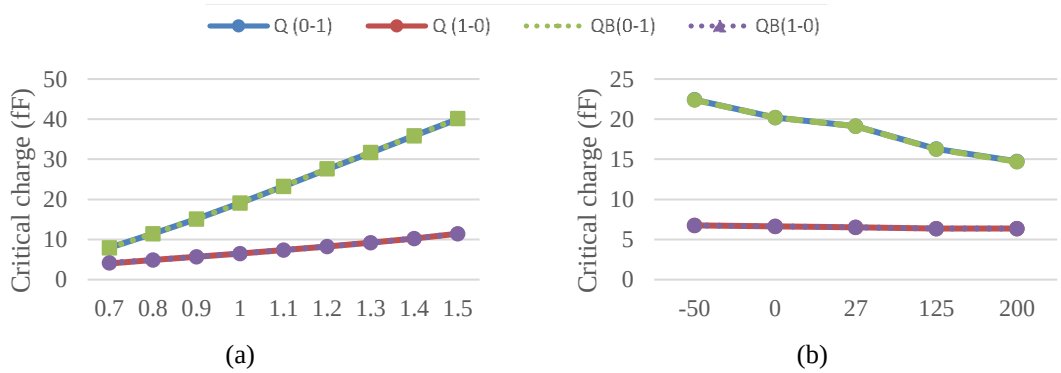


Figure 7. Graph of critical charge (fF) of 6T SRAM in hold state against; (a) voltage (V) and (b) temperature (ºC)

3.3. Transmission gate SRAM read state

The two nodes vulnerable to single event upsets are the memory storage nodes Q and QB in the inverter loop of the 6T SRAM [22]. To evaluate the sensitivity of the proposed SRAM cell, a double exponential current source as was defined in the previous section is injected into the storage nodes. Figure 8 presents a graph illustrating the critical charge of the nodes Q and QB of the proposed SRAM in the read state, where a range of supply voltage and temperature is manipulated to observe its effect on the critical charge. The nodes Q and QB are tested while they are holding the data states "0" and "1". With reference to Figure 8(a), the critical charge increases as the supply voltage rises as the driving current and the node capacitance increases in turn. The critical charge to induce a change from data state 0-1 from 0.7 V to 1.5 V,

the nodes Q and QB experience an increase of 48.05% and 48.36% respectively. The critical charge for the state change for 1-0 in the nodes Q and QB increases from 42.49% and 42.59% respectively. One notable difference between the nodes holding "0" and the nodes holding "1" is that the critical charge for the latter is significantly smaller than the former. This is due to the sizing dependant nature of the SRAM, with the PMOS being sized smaller than NMOS in order to maintain a smaller pull up ratio to avoid unintentional overwriting of data during read operation [23], [24].

When the proposed circuit was subject to temperature variation as shown in Figure 8(b), an increase in temperature brought with it a decrease in the critical charge, displaying an increased weakness to single event upsets at higher temperatures. From -50 ºC to 200 ºC, the critical charge for flipping a bit from "0" to "1" for nodes Q and QB decreases by 42.2% and 42% respectively. To flip the "1" to "0" on the other hand, the critical charge decreases by 14.54% and 14.22% for node Q and QB respectively. The increased temperature brings with it decreased device carrier mobility resulting in a decrease in critical charge [25].

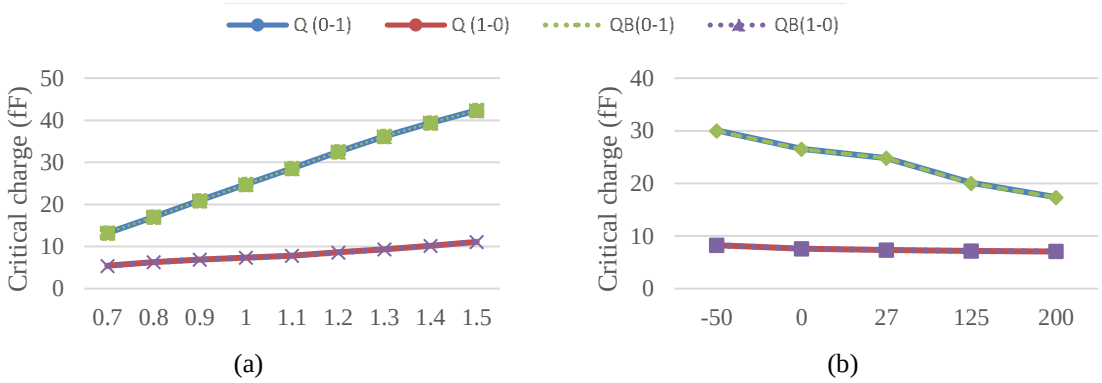


Figure 8. Graph of critical charge (fF) of proposed SRAM in read state against; (a) voltage (V) and (b) temperature (ºC)

3.4. Transmission gate SRAM hold state

The hold state presents a similar trend in critical charge for voltage and temperature as that of the read state as shown in Figure 9. The critical charge for the hold state is higher than the read state because the nodes are equated to the supply voltage [26]. The critical charge against the voltage and temperature for the SRAM hold state is shown in Figures 9(a) and (b), respectively. The increase of voltage in turn increases the critical charge of the nodes Q and QB regardless of which state is being held, albeit by a smaller degree in the case that the node is holding a "1", due to the smaller sizing of the PMOS transistor [27]. The critical charge for flipping a bit from "0" to "1" for nodes Q and QB increases by 54.6% and 54.9% respectively as the voltage is increased. This is to be expected as the node becomes more difficult to be affected by the injected transient current with a higher supply voltage. On the other hand, in order to flip a "1" to "0" the nodes Q and QB experience a rise in critical charge of 39% from the range of 0.7 V to 1.5 V.

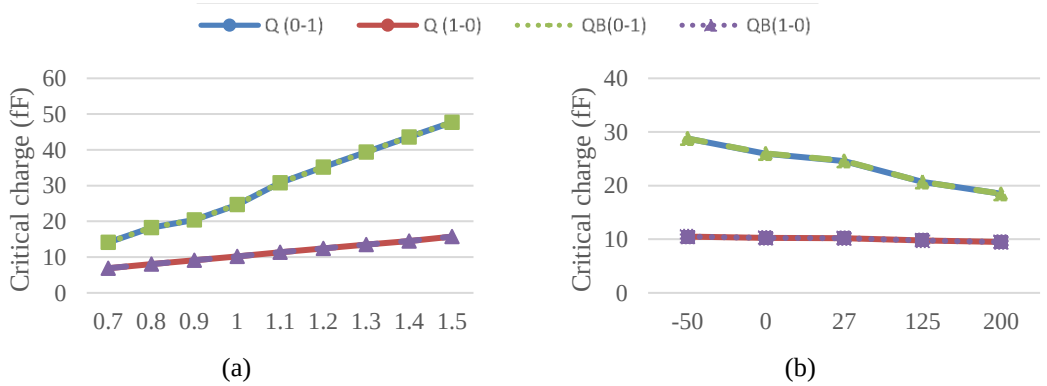
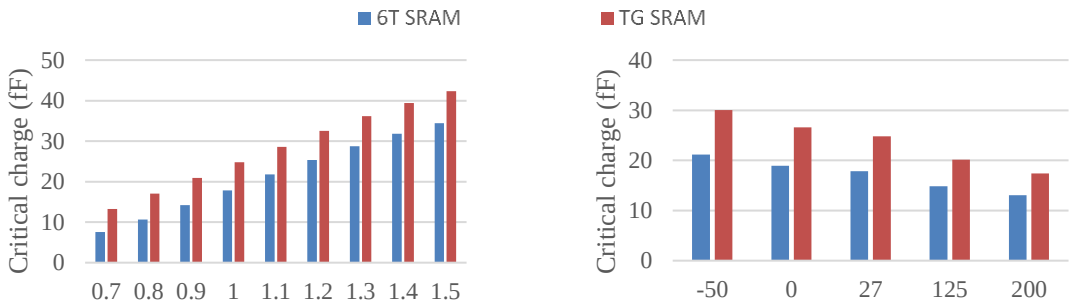


Figure 9. Graph of critical charge (fF) of proposed SRAM in hold state against; (a) voltage (V) and (b) temperature (°C)

In the case of the temperature variation in the Figure 9(b), the trend is similar to the temperature variation observed from the read state simulation. The critical charge to flip from "0" to "1" for node Q and QB decreases by 35.77% from -50 ºC to 200 ºC. On the other hand, the critical charge for the node Q and QB to flip the bit from "1" to "0" experiences a decrease of 9.55% and 9.67% respectively. As a consequence, the higher temperature levels has resulted in a system that is weaker to the effects of single event upsets. From read to hold state, the critical charge of the TG SRAM at 0-1 and 1-0 increases by 12.68% and 41.5% respectively for the voltage level 1.5 V. At 0.7 V the critical charges at 0-1 and 1-0 increases by 6.7% and 26.16% respectively from read to hold state.

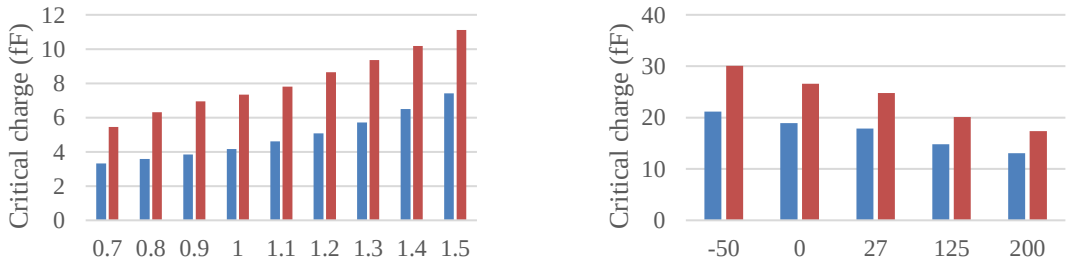
3.5. Performance comparison

In Figures 10 and 11, the critical charges of both the TG SRAM and 6T SRAM in read state with voltage and temperature variation. The critical charge of the TG SRAM has improved critical charge over the conventional 6T SRAM in both the read and hold states. In Figure 10(a), the voltage variation for 0-1, the lowest voltage level of 0.7 V shows the critical charge of the TG SRAM is higher than the 6T SRAM by 75%. At the point 1.5 V, the critical charge is improved by 22.9%. As the critical charge is higher at higher voltage levels, the increase in critical charge post mitigation is relatively lesser. The rise in critical charge is more apparent when the supply voltage is smaller. The TG SRAM presents better critical charge when subject to temperature variation than its conventional 6T counterpart. As shown in Figure 10(b), at the temperatures -50 ºC and 200 ºC, the critical charge of the TG SRAM in comparison to the 6T SRAM for 0-1 is increased by 41.9% and 33% respectively. In the voltage variation, TG SRAM delivers an increased critical charge for both the nodes holding "0" as shown in Figure 10(a) and "1" Figure 11(a). In Figure 11(a) for 1-0, at the voltage point 0.7 V the TG SRAM critical charge presents an improvement of 64.91%. The critical charge is improved by 50% when the voltage supply is set at 1.5 V. For 1-0, the critical charge is improved by 92% at -50 ºC and 81% at 200 ºC as presented in Figure 11(b).



(a) (b)

Figure 10. Graph of critical charge (fF) of proposed SRAM and 6T SRAM for 0-1 in read state against; (a) voltage (V) and (b) temperature (°C)



(a) (b)

Figure 11. Graph of critical charge (fF) of proposed SRAM and 6T SRAM 1-0 in read state against; (a) voltage (V) and (b) temperature (°C)

Figures 12 and 13 compare the critical charges for TG SRAM against 6T SRAM when voltage and temperature variation is applied during the hold state. When the supply voltage is adjusted to 0.7 V and 1.5 V, the critical charge improvement over the 6T SRAM for 0-1 was observed to be 77.87% and 19.23%

respectively as seen in Figure 12(a). For temperatures of -50 ºC and 200 ºC, the critical charge is improved by 28% and 23% respectively in Figure 12(b). In order to flip the bit from 1 to 0, the critical charge has been been improved by 71.5% and 37.49% for the voltages 0.7 V and 1.5 V as can be observed in Figure 13(a). The critical charge at the temperature points -50 ºC and 200 ºC see an improvement of 55% and 48.99% respectively as in Figure 13(b). The performance of the transmission gate filter was also compared to other similar strategies that were designed to withstand the effects of single event upsets. The comparison of performances have been visualised as in Table 1.

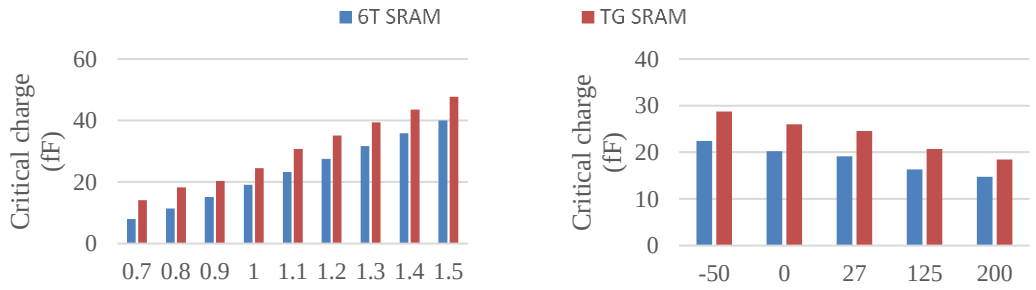


Figure 12. Graph of critical charge (fF) of proposed SRAM and 6T SRAM 0-1 in hold state against; (a) voltage (V) and (b) temperature (ºC)

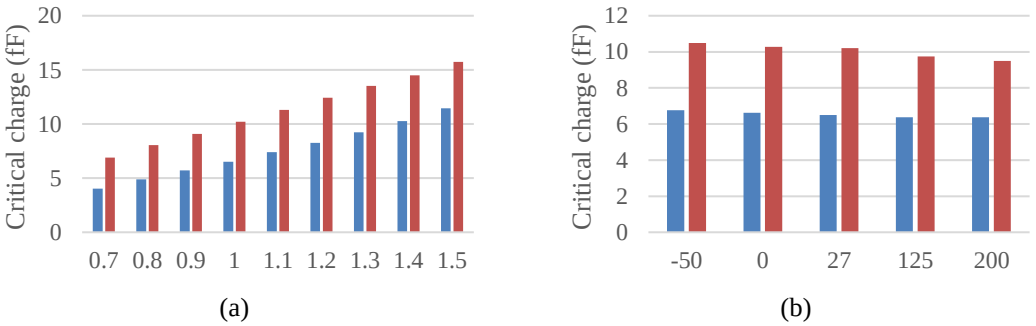


Figure 13. Graph of critical charge (fF) of proposed SRAM and 6T SRAM 0-1 in hold state against; (a) voltage(V) and (b) temperature (ºC)

Table 1. Critical charge improvement of various design strategies

Technique	Critical charge improvement (%)
Radiation hardening by design [28]	81.88
CR optimizing [29]	24
Transistor gate size optimizing [30]	58
Transmission gate transient filter	88.63

The transmission gate transient filter as proposed in this paper makes use not only of the stability of the selected CR in order to provide a high resistance in corruptibility during the read process but also in optimised dimensions in order to ensure greater robustness against current transients that occur in the instance of single event upsets. Radiation hardening by design is a strategy that has been proposed to design a 14T SRAM which has dedicated wordlines for the read and write states, thus increasing the stability of the read and hold states, allowing for a higher resistance against single event transients against similar design by achieving a critical charge increase of 81.88% [28]. However, the area overhead is significant in order to achieve the aforementioned level of stability. In comparison, the transmission gate transient filter results in a much lower transistor count, all the while achieving a critical charge improvement of 88.63%.

Furthermore, efforts have been made to achieve an increase in critical charge via the optimisation of CR in SRAM and size optimisation in transistors [29], [30]. However, it is apparent that the use of the proposed method, which makes the combined use of size, CR optimisation as well as the utilisation of the transmission gate transient filter in unison to provide greater overall protection. The method proposed has

been designed to prioritise the increase in protection against the data corrupting effects of the current transient while taking into account the consideration for area overhead and cost. It must also be noted that while the increase in critical charge acquired from CR and transistor gate sizing is substantial, the combination of these techniques as well as the use of transmission gates results in a higher critical charge improvement of 88.63%, leading to a great resilience against data corruption by single event upset.

Thus, the proposed method has provided a more desirable degree of protection from single event upset as indicated from the critical charge improvement in comparison to other existing methods as shown in Table 1. Moreover, the proposed method has a much reduced area overhead and design cost in terms of transistor sizing and number of transistors used. The use of the proposed method culminated in an SRAM cell that is robust against soft errors and designed with optimal sizing.

4. CONCLUSION

This paper proposed an improved SRAM cell with transmission gate that has an increased resistance against soft error. The nodes Q and QB are injected with soft error that with current pulse with characteristics of single event upset to observe the critical charge of needed to flip the output from 1-0 and 0-1. The parameters of supply voltage and temperature were varied over a range to observe the effects on the critical charge of the cell, and to gauge its shift to the critical charge. The increase in voltage was observed to induce an increase in critical charge, with the inverse for temperature. The simulation presented an improvement of the critical charge in both the nodes Q and QB when holding the state "0" and "1" in when subject to temperature and voltage variation in comparison to the conventional 6T-SRAM. The TG SRAM has a greater effect on the critical charge in response to temperature variation than the voltage variation. Furthermore, the findings of this study has devised a sizing for the transmission gate that provides a greater protection against single event upsets, improving upon the critical charge of the 6T-SRAM by 88.63%. This contribution is significant in that a versatile transient filter can be applied to storage nodes in SRAMs and improve the soft error robustness of the SRAM cell. These findings display that the use of transmission gates could be a useful mitigation tool against soft errors in the design of CMOS memory systems, opening up a new avenue for designers in increasing soft error robustness. As the higher critical charge provides greater protection against data corruption, the final product is thus more robust against soft errors. Future works could explore the effectiveness of the proposed filter in various SRAM configurations at other technology nodes.

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