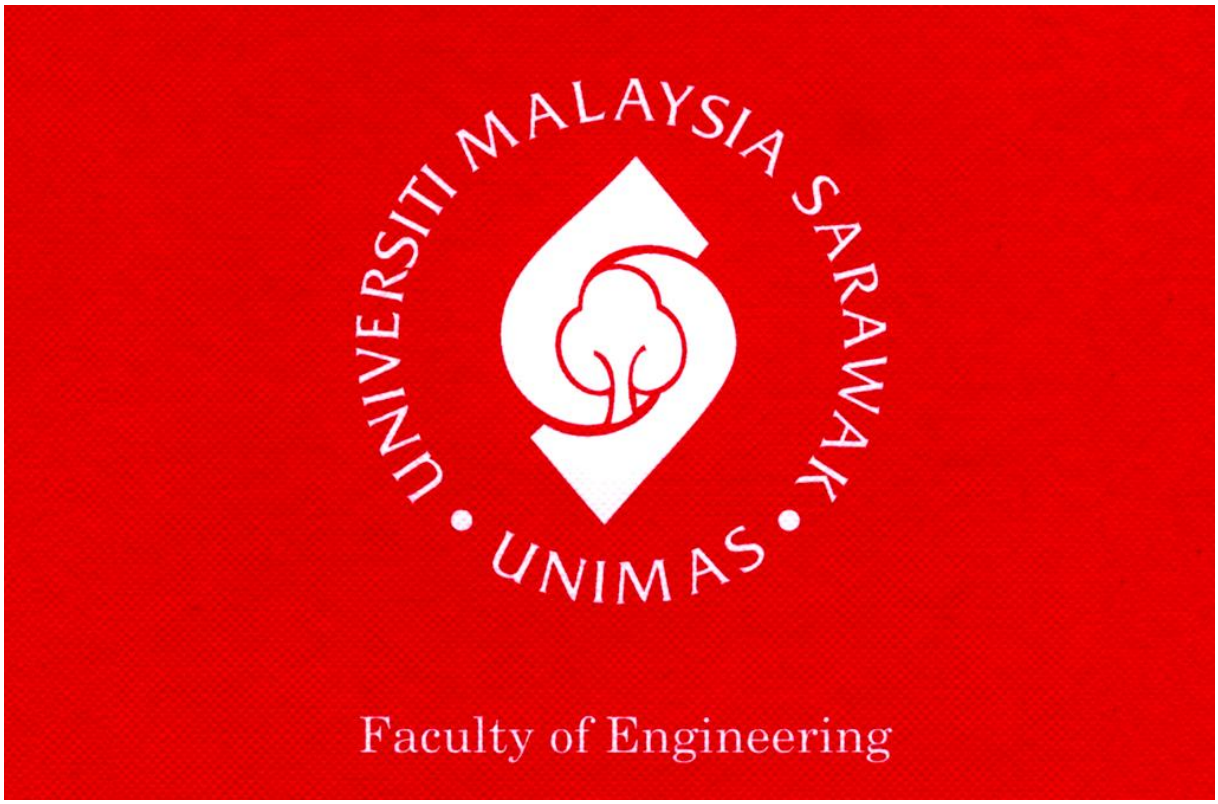

DESIGN OF LOW VOLTAGE CMOS TRISTATE BUFFER

Nurul Huda binti Zulkifli

Bachelor of Engineering with Honours

(Electronic and Telecommunication Engineering)

2010

UNIVERSITI MALAYSIA SARAWAK

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Student Name : Nurul Huda binti Zulkifli

Matric No : 17052

has been read and approved by:

_____ _____

Mdm. Sharifah Masniah Wan Masra Date

(Supervisor)

DESIGN OF LOW VOLTAGE CMOS TRISTATE BUFFER

NURUL HUDA BINTI ZULKIFLI

This project is submitted in partial fulfillment of
The requirements for the degree of Bachelor of Engineering with Honours
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Faculty of Engineering
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Dedicated to my beloved family and friends.

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ABSTRAK

CMOS tristate buffer banyak digunakan dalam sistem elektronik. Dengan meningkatnya pengggunaannya, juga menuntut bahawa buffer yang beroperasi di kelajuan tinggi. Jadi kelajuan tinggi CMOS tristate buffer direkabentuk. Sistem kelajuan tinggi adalah mudah untuk dilaksanakan, tetapi untuk kelajuan tinggi dengan sistem voltan rendah yang sukar dicapai. Kerana voltan yang digunakan adalah rendah, kuasa yang digunakan juga akan menjadi rendah. Tujuan projek ini adalah untuk merekabentuk suatu tristate buffer voltan rendah yang boleh menggerakkan beban kapasitif lebih besar. Masalah yang timbul adalah bagaimana untuk mengawal throughput kerana dalam kebanyakan kes jika voltan sistem diturunkan, kelajuan sistem akan menurun juga. Dengan melakukan pensaizan transistor terhadap litar kelajuan tinggi itu, voltan bekalan yang digunakan dalam litar ini diturunkan dari voltan bekalan litar kelajuan tinggi. Nilai optimum yang dipilih untuk voltan bekalan adalah 1.6 V sementara nilai yang dipilih untuk beban kapasitif adalah 10 pF. Disebabkan nilai voltan yang digunakan semakin rendah, pada masa yang sama didapati PDP dan EDP juga menurun, sementara kelajuan tinggi dikekalkan.

ABSTRACT

CMOS tristate buffer are widely used in electronic systems. As the increasing of its usage, it is also demanding that the buffer is operating in high speed. So the high speed CMOS tristate buffer is designed. High speed systems are easy to be implemented, but for a high speed with low voltage system are difficult to achieve. As the voltage used is low, the power consumption will be also low. The objective of this project is to design a low voltage tristate buffer that can drive a larger capacitive load. The problem is how to maintain the throughput while in most cases, lowering voltage of the system will lowering the system speed too. By applying transistor sizing to the high speed circuit, the supply voltage used in this circuit is lowered from the high speed design. The chosen optimum value used for supply voltage is 1.6 V while chosen value for capacitive load is 10 pF. As the value of the supply voltage is getting lower, it is shown at the same time that the Power Delay Product and Energy Delay Product also decreasing while maintained the high speed.

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ABBREVIATIONS

AC	-	Alternating current
ASIC	-	Application-Specific Integrated Circuit
BiCMOS	-	Bipolar Complementary Metal Oxide Semiconductor
BSIM	-	Berkeley Short-Channel IGFET Model
CMOS	-	Complementary Metal Oxide Semiconductor
COS-MOS	-	Complementary-Symmetry Metal-Oxide-Semiconductor
DC	-	Direct Current
EDP	-	Energy Delay Product
I/O	-	Input/Output
IC	-	Integrated Circuit
MOS	-	Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	N-type Metal Oxide Semiconductor
PDP	-	Power Delay Product
PMOS	-	P-type Metal Oxide Semiconductor
TTL	-	Transistor-Transistor Logic
VLSI	-	Very Large Scale Integration
W/L	-	Width/Length

CHAPTER 1

INTRODUCTION

1.1 Introduction

Recently, all digital circuits are demanded to operate with low power consumption as power dissipated by electronic circuit affect the portability and size of electronic systems. The most important technology consideration in minimizing power consumption for digital systems is the threshold voltage and its control which allows the reduction of supply voltage without significant effect on logic speed.

Since CMOS circuits do not dissipate power if they are not switching, a major focus of low power design is to reduce the switching activity to the minimal level required to perform the computation. This can range from simply powering down the complete circuit or portions of it, to more sophisticated schemes in which

the clocks are gated or optimized circuit architectures are used which minimize the number of transitions [1].

An important attribute which can be used in circuit and architectural optimization, is the correlation which can exist between values of a temporal sequence of data, since switching should decrease if the data is slowly changing (highly correlated) [1].

So for achieving this goal, the effect of sizing and supply voltage on the circuit is extensively considered. The optimization to minimize area at all costs has only been secondary to the fixation on increasing circuit speed, but this should be examined with respect to its effect on power consumption. Energy Delay Product (EDP) and Propagation Delay Product (PDP) have been the main objectives of this research as it is compromise between the attempt to reduce the energy and time consumption.

The tristate buffer are extensively used as a bus in digital systems such as microprocessor, ASIC and memory. When one device is sending on the bus, another sending device should be disconnected. This can be achieved by setting the output buffers of those devices in high impedance state (Hi-Z) that effective disconnects the gate from output wire. Such a buffer has three possible states that are 0, 1 and Hi-Z therefore called tristate buffer. Owing to a bundle of wires connected to a bus, a large capacitive load driving capability is one of the most importance properties of tristate buffer [2].

CMOS is more attractive than BiCMOS in electronic system because of its simplicity, low power consumption and optimization of purity in circuit compared to BiCMOS circuit which utilizing CMOS and BJT in the same circuit [3]. For this reason, a low voltage tristate buffer based on CMOS technology that can drive larger capacitive load that is suitable for driving a data bus will be designed.

1.2 Problem Statement

Designs of high speed tristate buffer have been developed by some researchers. However, only [1] have developed high speed and low voltage tristate buffer using BiCMOS with large capacitive load driving capability. Recently attention on BiCMOS circuit technology has increased because of their high speed and driving capability over CMOS. However, electronic industry still chooses CMOS over BiCMOS because BiCMOS process complexity that contributes to higher cost and longer fabrication cycle time. Thus, a low voltage CMOS tristate buffer that can drive larger capacitive load for driving a data bus will be designed.

Problems arise with building low voltage products to be compatible with existing products that utilize a higher power supply potential.

One problem exists with the compatibility of conventional input/output (I/O) buffers using CMOS low-voltage processing technology. If conventional output buffers are used in CMOS products operating with a low voltage supply, then current leakage problems may arise when higher voltages are driven into the output pad

while the buffer is in a tristate mode. Obviously, current leakage problems are undesirable in an integrated circuit, especially in cases where the magnitude of the leakage violates accepted I/O bus standards [4].

Other problems also exist when tristateable output buffers operating from a low voltage supply are connected to a higher voltage bus. In addition to the leakage problem, there are two long-term reliability issues to consider. These problems are commonly referred to as “hot electron reliability” and “p-device stability” [4].

Hot electron reliability denotes the phenomenon wherein the operating performance of a transistor degrades due to a build up of trapped carriers in the gate oxide region. Because electron carriers have a higher mobility than hole carriers, this problem is more pronounced for n-channel devices as compared to p-channel devices [4].

The performance of a transistor degrades as the electric field of the trapped carriers interact with the electric field applied at the gate of the transistor. Hot electron reliability is a probabilistic model where the probability of a carrier being trapped in the oxide is a function of the energy of the carrier as it passes through the channel of the transistor. At the operating point of saturation devices have the highest probability of injecting carriers into the gate oxide. Among the factors that determine if a transistor will experience hot electron reliability problems include frequency of switching, size of load, operating temperature, driving potential, device channel length, device channel width, the rise/fall times of the signal on the gate, and the expected lifetime of operation of the transistor in the field [4].

Another long-term reliability risk, referred to as p-device stability, involves the undesirable shift in the threshold voltage when excessive electric fields have been applied across the gate oxide of a p-channel transistor. Note that n-channel devices are also susceptible to a shift in their threshold voltage as a result of excessive electric fields being experienced across their gate oxide. However, p-channel devices are usually more sensitive to this phenomena [4].

Other problem is that, how to design a low voltage supply without degrade the performance because it is extensively known that the speed degradation at low supply voltage is the major limitation factor of both CMOS and BiCMOS in submicron technologies [2].

1.3 Project Objectives

In this project, the following goals will be achieved:

1. To design and simulate using Pspice a low voltage tristate buffer that can drive larger capacitive load.
2. To obtain lower EDP than previous researchers' EDP.
3. To find the optimized tradeoff value between voltage and speed of CMOS tristate buffer.

1.4 Project Scope

This project is a research on how to design a low voltage CMOS tristate buffer while maintained or improved speed of the previous proposed design. The new proposed design will improve recent driving capability where wasted power can be reduced.

1.5 Report Structures

This report details overall process in developing the project starting from the early idea of development, circuit development planning, software simulation until report writing. This report is divided into five chapters including introduction; literature review; methodology; results and discussion; and conclusion and recommendation. The brief information of each chapter is described as below:

Chapter 1 provides background information, problem statement and objectives of the project. It also provides scope of the project, project planning and project structures.

Chapter 2 summarizes and reviews onto the overall studies and researches work. Preliminary literature search included existing issues such as design of high speed and low voltage tristate buffer using BiCMOS and minimizing power consumption in digital electronic circuit are explained in detail.

Chapter 3 discusses the methodology and focuses on the use of Pspice simulator to obtain the result to be achieved. The first part of this chapter concentrates about the circuit development methodology. The second part shows the proposed design circuit as well as the circuits of conventional design and high speed design to be compared. The descriptions of the circuits are also have been discussed.

Chapter 4 exhibits the results and data obtained from the Pspice simulation. It carries out analysis and discussion onto the data. It also examines whether the simulation results fulfil the predicted or expected results as mentioned in the early part of the project. Besides, different approaches and testing taken out to examine the project in achieving its objectives are listed in details.

Chapter 5 summarizes the overall finding of the project. The problems faced throughout the project are discussed too. In addition, further investigation which can be implemented or future improvement of the project is being discussed.

Appendices and references are also included at the end of the report.

CHAPTER 2

LITERATURE REVIEW

2.1 Basic Concept of CMOS

Complementary metal-oxide-semiconductor (CMOS) is a technology for making integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for a wide variety of analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Frank Wanlass successfully patented CMOS in 1967 (US Patent 3,356,858) [4].

CMOS is also sometimes referred to as complementary-symmetry metal-oxide-semiconductor (or COS-MOS). The words “complementary-symmetry” refer to the fact that the typical digital design style with CMOS uses complementary and

symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions [4].

Two important characteristics of CMOS devices are high noise immunity and low static power dissipation. CMOS dissipates power only when the transistors in the CMOS device are switching between ON and OFF states. This shows that CMOS devices do not produce as much waste heat as other logic devices such as transistor-transistor logic (TTL) and NMOS logic, which uses all n-channel devices without p-channel devices [4].

Other than that, CMOS is better than bipolar junction transistor (BJT) in the aspect of power dissipation, noise margin, packing density, a good switch and also the ability to integrate large and complex circuits and functions with high yield. This is the reason why CMOS become the most used technology to be implemented in VLSI chips [3].

From all of the reasons above, we can see why CMOS is preferred to be used in most digital logic circuits rather than other logic circuits. Even though BiCMOS become technology choice recently, CMOS still become electronic market choice. Inverter and tristate buffer will be explained in the following section.