Performance Analysis of Distance-Based Wireless Transceiver Placement for Wireless NoCs with Deterministic Routing

Asrani Lit†, **Shamsiah Suhaili**, **Nazreen Junaidi**,
Shirley Rufus, and **Nurul Izzati Hashim**, Non-members

ABSTRACT

This research analyzes the impact of wireless transceiver subnet clustering on a hundred-core mesh-structured WiNoC architecture. The study aims to examine the effects of distance-based wireless transceiver placements on transmission delay, network throughput, and energy consumption in a mesh Wireless NoC architecture with a hundred cores, particularly under the X-Y, West-First, Negative-First, and North-Last routing strategies. This research investigates the impact of positioning radio subnets at the farthest, farther, nearest, and closest positions within an architecture featuring four wireless transceivers. The Noxim simulator was used to simulate the analyzed wireless transceiver placements on the hundred-core mesh-structured WiNoC designs, with the objective of validating the results. The architecture with the wireless transceiver positioned at the midway proximity (nearer and further) delivers the best performance, as evidenced by the lowest latencies for all evaluated deterministic routing algorithms, corresponding to the simulation outcomes.

Keywords: Distance-based Optimization, Wireless Transceiver, Optimal Placement, Wireless Network-on-Chip, Deterministic Routing Algorithm

1. INTRODUCTION

In the preceeding years, there has been a growing importance in the utilization of on-chip interconnect topologies as a means of communication for chip multiprocessors. This trend is supported by various studies, including those conducted in [1–3]. Recent advancements in semiconductor technology have enabled the successful integration of integrated circuits incorporating even more processing components into a chip multi processor architecture. Furthermore, several integrated chip project using Network-on-Chip (NoC) technology, comprising of many processing cores, have been developed and utilized in various prototypes such as SCORPIO [4], MIT RAW [5], Xeon Phi [6] and Intel TILERA [2].

The issue of wire delay poses a notable obstacle for on-chip network systems, for the most part in the context of extensive on-chip interconnects, due to its potential to significantly affect the overall performance of the network. The standard wired Network-on-Chip (NoC) infrastructure is facing constraints due to the growing number of computing cores, as it heavily depends on multiple hop far reaching communication. Consequently, this leads to an architectural design that uses a greater amount of power and has elevated latency. Therefore, in order to tackle the issues related to significant propagation delay and multiple-hop long-distance communication between processing cores, Wireless NoCs introduce flexibility in communication by enabling direct links between distant nodes, thus potentially reducing hop count and latency.

The challenge posed by wire delay is importance in chip-based network architecture, especially while addressing expansive on-chip communication systems, as it can significantly affect the entire network capabilities and performance [7, 8]. As quantity of processing cores continues to grow, the traditional wired NoC architecture faces limitations due to its dependence on long-distance multi-hop communication. Consequently, this results in an architecture that use more power and demonstrates increased latency. Therefore, to tackle challenges related to elevated latency in signal propagation and long-distance multi-hop communication between processing cores, computer architects and researchers have introduced the design of Wireless NoC (WiNoC) interconnect as a viable solution [9, 10].

This approach requires the integration of one-hop wireless transmission to allow far reaching communication among processor cores, as referenced in multiple studies [11–16] for its efficacy and scalability. The WiNoC setup incorporates integrated transceivers, facilitating an immediate wireless channel for the transfer of packets over long distances on the chip, as supported by several research findings [12, 17, 18]. The effectiveness of the WiNoC framework is significantly influenced by several importance network features, such as the arrangement of its topology, the management of data

Manuscript received on November 8, 2023; revised on March 5, 2024; accepted on March 29, 2024. This paper was recommended by Associate Editor Nutapong Somjit.

The authors are with Department of Electrical and Electronics Engineering, Universiti Malaysia Sarawak (UNIMAS), Malaysia.

†Corresponding author: lasrani@unimas.my

Digital Object Identifier: 10.37936/ecti-eec.2024222.251668