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SOFT ERROR MITIGATION IN MEMORY SYSTEM

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Abstract

Technology downscaling has increased the sensitivity of circuitry to being corrupted by single event upsets. To provide more solutions for the issue, a method of error detection and correction is provided in this study. The double exponential model was used to simulate the single event upset current transient. The amplitudes of the transient current from the single event upset were varied until a change in logic value is achieved. A single rail with inverter latch (SIL) circuit configuration is injected in three vulnerable nodes to formulate their respective soft error sensitivities, with the parameters of temperature and voltage supply varied to observe their effects on the critical charge of each node. The temperatures were ranged from -50ºC to 200 ºC, while the supply voltage was varied from 0.7 V to 1.5 V. Decreases in temperature from the range of 200ºC to -50ºC cause the critical charge to increase. Critical charge increases with voltage supply increase from 0.7 V to 1.5 V. A shadow latch was implemented in Cadence and Quartus for error detection and correction. The shadow latch was able to successfully detect the presence of an error and restore the original data from voltages of 0.8 V to 1.2 V.

Keywords: Error correction, Error detection, Latch, Soft error.

1. Introduction

Soft errors have been an increasing worrying problem with the trend of downscaling technology. Soft errors are the result of interactions of energised particles interacting with the electrons in electronic circuitry [1]. There are many sources of these energised particles against which designers must take into account when designing circuits. These include alpha particles, cosmic neutrons, and radiation from the interactions of boron and cosmic neutrons. Alpha particles as a soft error source are borne from the decay of radioactive impurities [2, 3]. Electronics in close proximity to nuclear reaction have little in the way of protection from high energy neutrons and are prone to the occurrence of soft errors [4]. Furthermore, space environments in which high performance equipment used in satellites and aerospace fields, are exposed to a spectrum of ionised particles must also operate in a soft error rich environment.

Secondary particles can be formed when cosmic rays interact with the atmosphere. Neutrons are the primary source of soft errors at the terrestrial level from cosmic rays [5]. Another primary source of radiation in semiconductors is the interaction of cosmic neutrons with boron, which consequently emits alpha particles. These sources are capable of producing soft errors in electronics in vulnerable regions in devices via charge generation, which is the result of the traversal of a particle across a susceptible circuit node. Transistors in the "off" state in CMOS circuitry are highly prone to single effect upsets. Single event upsets can be created by a particle strike in the sensitive region of an NMOS or PMOS transistor. There will then be a current pulse which produces charge, the amount of which can produce a single event transient if it were to reach the critical charge (Q_{crit}). If an energised particle that has also been ionised within close proximity to a vulnerable circuit node, electron-hole pairs can be formed along its trajectory. This can result in charge collection event that will generate a current transient. There are numerous methods that have been used in soft error mitigation, several of which will be discussed in the next section.

In this paper, we used a C-element circuit which is single rail with inverter latch configuration (SIL) as our case study and we demonstrated the technique to detect and correct soft errors that occur in a system. SIL is chosen as case study for memory system and it hold the previous value if the two inputs are not equal.

2. Related Work

2.1. Radiation hardness by design

One method is by employing radiation hardening by design. This is done by implementing changes to a circuit at the design level for memory elements and can involve modifications to layout or circuit design. Pown and Lakshmi [6] proposed a 6T double gate tunnel field effect transistor static random access memory circuit. The design features a resistor and capacitor (RC) component attached between the data nodes of the SRAM, assists data recovery by dampening voltage transients and upping the critical charge. Similar implementations involve integration of resistor-capacitor filtering or selective redundancy for radiation mitigation [7].

The method of radiation hardness by design can also be applied to other existing techniques such as triple modular redundancy circuits [8]. The study provides a SEE-tolerant TMR circuit architecture for space applications. The proposed D-flip-