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Design of 3.1-10.6 GHz UWB CMOS Power Amplifier using Cascade Topology

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ABSTRACT

Power amplifier is an important component in the wireless communication system. Design of the power amplifier in UWB transceiver is challenging as the signal need to be transmitted over a wide bandwidth. Several criteria need to be fulfilled such as good linearity, good wideband matching, high efficiency and low power consumption. This paper presents the design of a power amplifier with 3.1-10.6 GHz using 0.18 µm CMOS technology for ultra-wide band application. The proposed power amplifier used three cascaded amplifier stages in order to achieve good gain and wide-band width. The results show that the proposed power amplifier design has an average gain of 7.28 dB, an input return loss less than -7.48 dB, an output return loss less than -4.782 dB, and group delay variation of ±151.9 ps is achieved over the entire band. A good input 1dB-compression point of 6.67 dBm and input third order intercept point of 0 dBm is achieved at 5 GHz.

1. Introduction

The rapid growth in modern technology, especially in wireless communication systems such as ultra-wideband (UWB), wireless personal area network (WPAN) and wireless local area network (WLAN) enabling users to communicate anywhere any time. This has become a necessity in our daily life. In February 2002, the Federal Communication Commission (FCC) has allowed the data transmission in the wide-ranging frequency of 3.1 to 10.6 GHz that allows data transmission at a higher rate of 100 to 500 Mbps with low power consumption [1]. As a result, the UWB has been considered as one of the most promising wireless technologies because of its ideal benefits such as low cost, high data rates, low power, low interference, and precise positioning.

Power amplifier is an important block in the wireless communication system. It is normally located at the final stage in the transmitter unit. It amplifies the signal and generates enough power

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to allow the signal to transmit over the required range. Power amplifier is one of the most challenging devices to design in UWB transceiver since it is required to transmit the signal over a wide bandwidth. It must meet several requirements such as good linearity, good wideband matching, high efficiency and low power consumption. Numerous UWB CMOS power amplifiers have been reported with frequency of 3.0–5.0 GHz, 3.0-7.0 GHz, 6.0–10.0 GHz and 3.1-10.6 GHz with various types of implemented topologies such as distributed amplifier, resistive shunt feedback and RLC matching, current-reused approach, common source inductive degeneration, current-reused technique, inter-stage wideband impedance transformer and stagger tuning [2-11]. Wideband matching in power amplifier design can be accomplished using distributed amplifiers, however, this topology consumes high power and large chip area [12]. Shunt-peaking technique is employed to provide wideband matching, but it affects the input and output matching. Resistive shunt feedback offers wideband matching and good input and output matching. This method results in a smaller chip area than other methods since it has less or no inductors. Inductive source degeneration has the potential to provide good input wideband matching as well as to enhance the linearity but lower the gain of the amplifier [9]. The advantage of using current-reused technique is to reduce power consumption, but it is quite difficult to meet the gain and wide frequency band from 3.1 to 10.6 [12]. In this paper, a design of 3-10.6 GHz UWB CMOS power amplifier by using cascade topology is proposed. The proposed UWB power amplifier implemented with 0.18 µm CMOS technology has obtained good parameters such as gain and linearity within the frequency of 3.1-10.6 GHz.

2. Methodology

The parameters for the proposed power amplifier design specifications are shown in Table 1 and the design is shown in Figure 1.

Table 1
Power amplifier design specification

Parameter	Specification
Frequency (GHz)	3.1-10.6
Gain (S_{21}) (dB)	>10
Input return loss (S_{11})	<-5
Output return loss (S_{11})	<-5
Reverse isolation, S_{12} (dB)	<-30
Input P1dB	>22
Output P1dB (dBm)	≈0
Group delay (ps)	<±100
Power consumption (mW)	<100