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Abstract

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This paper proposed a design of a modern FPGA-based Traffic Light Control (TLC) System to manage the road traffic. The approach is by controlling the access to areas shared among multiple intersections and allocating effective time between various users; during peak and off-peak hours. The implementation is based on real location in a city in Malaysia where the existing traffic light controller is a basic fixed-time method. This method is inefficient and almost always leads to traffic congestion during peak hours while drivers are given unnecessary waiting time during off-peak hours. The proposed design is a more universal and intelligent approach to the situation and has been implemented using FPGA. The system is implemented on ALTERA FLEX10K chip and simulation results are proven to be successful. Theoretically the waiting time for drivers during off-peak hours has been reduced further, therefore making the system better than the one being used at the moment. Future improvements include addition of other functions to the proposed design to suit various traffic conditions at different locations.

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Keywords

Metrics

Published in: [2011 IEEE International Conference on Computer Science and Automation Engineering](#)

Date of Conference: 10-12 June 2011

INSPEC Accession Number: 12121879

Date Added to IEEE Xplore: 14 July 2011

DOI: 10.1109/CSAE.2011.5952814

► ISBN Information:

Publisher: IEEE

Conference Location: Shanghai, China

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Design of FPGA-Based Traffic Light Controller System

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Abstract— This paper proposed a design of a modern FPGA-based Traffic Light Control (TLC) System to manage the road traffic. The approach is by controlling the access to areas shared among multiple intersections and allocating effective time between various users; during peak and off-peak hours. The implementation is based on real location in a city in Malaysia where the existing traffic light controller is a basic fixed-time method. This method is inefficient and almost always leads to traffic congestion during peak hours while drivers are given unnecessary waiting time during off-peak hours. The proposed design is a more universal and intelligent approach to the situation and has been implemented using FPGA. The system is implemented on ALTERA FLEX10K chip and simulation results are proven to be successful. Theoretically the waiting time for drivers during off-peak hours has been reduced further, therefore making the system better than the one being used at the moment. Future improvements include addition of other functions to the proposed design to suit various traffic conditions at different locations.

Keywords- FPGA; Traffic Light Control; intersections; traffic; peak hours; off-peak hours

I. INTRODUCTION

Field Programmable Gate Array (FPGA) is an Integrated Circuit (IC) that contains an array of identical logic cells that can be programmed by the user. The Altera FLEX10K provides high density logic together with RAM memory in each device. FPGA has many advantages over microcontroller in terms of speed, number of input and output ports and performance [1]. FPGA is also a cheaper solution compared to ASICs (custom IC) design which is only cost effective for mass production but always too costly and time consuming for fabrication in a small quantity.

Traffic light controller (TLC) is used to lessen or eliminate conflicts at area shared among multiple traffic streams called intersections; by controlling the access to the intersections and apportioning effective period of time between various users. The main goal of this project is to manage the traffic movement of four intersecting roads and to achieve optimum use of the traffic. In general, traffic lights of all main roads are controlled with a fix-time control system while the smaller roads are controlled autonomously by sensors.

During rush hours, when people are going to work or going back home, traffics are at the maximum capacity and without an effective TLC system, will almost always resulting in traffic jams. This problem arises due to the unbalance traffic flow from only certain directions on huge intersections, which is causing a major congestion on the affected directions and at the same time having an un-optimized use of traffic on the less congested direction. Approach has been made by putting the traffic policemen in charge of the traffic instead of the traffic lights during the peak hours thus showing the ineffectiveness of the system in the most demanding situation. This project aims to address this major flaw and hopefully come out with a better solution to the problem.

Many research works have been done on traffic light controller using different controlling methods. Chavan, Deshpande and Rana have developed TLC based on microprocessor and microcontroller. But, there is some limitation in this design due to no flexibility of modification on the TLC during real time [2]. Liu and Chen have designed TLC using Programmable Logic Controller (PLC) to replace the relay wiring, as a result making the design better [3]. Kulkarni and Waingankar have proposed a TLC design using fuzzy logic, which has the capability of mimicking the human intelligence [4]. This design has been implemented using MATLAB and showed that it can control the traffic flow more efficiently compared to the fixed time control [4]. El-Medany and Hussain have implemented FPGA-Based 24-hour TLC that manage traffic movement of four roads and reached maximum utilization of the traffic during rush hour and normal time [1]. Shi, Hongli and Yandong have designed an intelligent TLC that can be applied both in common intersections and multiple branches intersections based on VHDL [5].

The use of VHDL is preferred especially for FPGA design because VHDL can be used to describe and simulate the operation of digital circuits ranging from few gates to come complex one [6]. In this project, the TLC will be design based on VHDL using QUARTUS II and implemented in hardware by using Altera FLEX10K chip.

II. ROAD STRUCTURE

One of the busiest traffic lights in Kuching city, Malaysia has been identified and used as the reference model for the design. Road structure of the traffic

intersection is shown in Fig. 1. In this structure, there are six traffics, represented by T1, T2, T3, T4, T5 and T6 to be controlled. T1 and T2 have been identified as the main road for the first junction while T4 and T6 are for the second junction. The last two traffic lights, T3 and T5 are the smaller roads. The traffic flows are symbolized by the arrows in the Fig. 1.

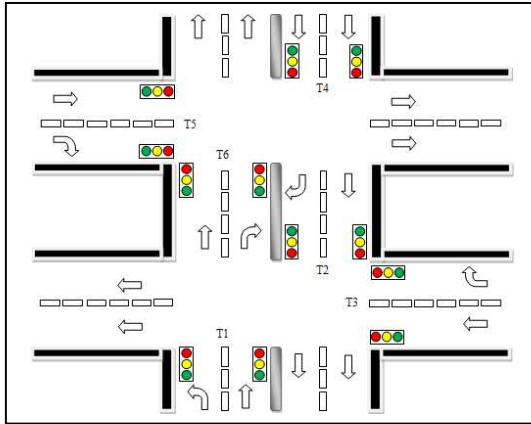


Figure 1. Road Structure

A. TIMING Setting

Time is an important criterion that must be set accurately and wisely, so that any dangerous situations, for example car accident can be avoided at the intersection. The timing settings for the TLC are as follows:

- **Green**
For main roads T1, T2, T4 and T6 are 32s (peak) / 16s (off-peak) while for narrow road T3 and T5 are 16s (peak) / 8s (off-peak).
- **Amber**
For all roads and during both peak and off-peak are 4s.
- **Red**
For all roads and during both peak and off-peak are 2s.

Fig. 2 displays the control method for the TLC during peak hour. It can be observed from this figure that the timing settings used is fixed time approach. Fixed time method is the most popular and old method that has been widely used in most of the TLC setting worldwide. The proposed design differs from the existing one in terms of the timing method. Although fixed time approach is used during peak time, alternatively during off-peak hour, inputs from sensors are used to determine the cycle of traffic lights. When both sensors (Sensor 1 and Sensor 2) are activated, the cycles are the same as Fig. 2 except that timing for green light will be less: for T1, T2, T4 and T6 the setting is 16s while for T3 and T5 it will be reduced to 8s.

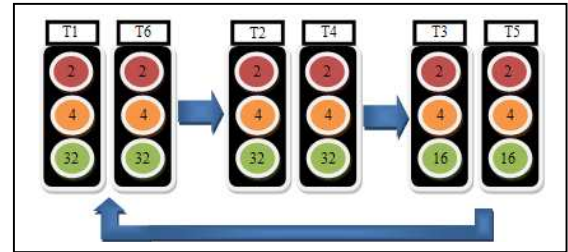


Figure 2. The control scheme (fixed-time) during peak hour

At a condition where only Sensor 1 is being set off, other cycles are the same as in Figure 2 except that T3 and T5 cycle will be replaced by T3 and T6, and both will turn green for 8s. When only Sensor 2 is triggered, cycles are similar to that during only Sensor 1 is activated except that in the last cycle flow, T2 and T5 will turn green instead of T3 and T5. At a time when both sensors are not activated, the cycles for T3 and T5 will be skipped.

B. VHDL Model

Fig. 3 shows the VHDL model of the controller. The model consists of:

- **CLOCK**: System clock
- **RESET**: System reset
- **PEAK**: Represents peak hour (1) and off-peak hour (0)
- **OUTPUT (17 DOWNT0 0)**: All represents the six traffic lights (time three different output combination) that the system is going to control.
- **SENSOR1 and SENSOR2**: Represent the two sensors used to detect the presence of car at the narrow road, T3 (Sensor1) and T5 (Sensor2).

In terms of system implementation, the approach is to develop a low cost, high efficiency TLC system. El-Medany and Hussain suggested every intersection to be equipped with sensors [1]. In contrast, this system only requires sensors to be present at the small roads where the traffic is not heavy thus reducing significant amount of component needed. However, this system is not solely dependent on the sensor input, as it is also equipped with a clock that is used to set the “peak hour”. This is the period where both sensors will be temporarily disabled and the traffic is controlled by a fixed-time system. This allows for many possible customization of the system to suit various traffic conditions in different types of intersection. In comparison, Liu and Chen have designed a TLC system using six timers and two specials for a very specific scenario [3]. This system has the advantage in terms of flexibility and can be applied to various intersections with different traffic conditions.

III. RESULTS AND DISCUSSION

Timing simulation is one way of verifying result of the design. Timing simulation waveforms shown in Fig. 4 – 8 show the outputs of the designed TLC.

The outputs of TLC during peak hour are shown in Fig. 4. For this project, peak-hour periods are set between

0700 – 0900, 1200 – 1400 and 1700 – 1900 hours. Both sensors are disabled and the fixed-time system flows as follows. First cycle initiated with T1 and T6 are green whilst others are all red. After 32s, T1 and T6 will change to amber for 4s and then red for 2s while others remained red. Second cycle begins with both T2 and T4 turn to green for 32s, subsequently amber for 4s and lastly red for 2s; others are red all the time. Third cycle starts when traffic lights T3 and T5 (at narrow roads) turn green for just 16s, followed by amber for 4s and in the end red for another 2s; others remained red. The first cycle will be repeated again.

Fig. 5 shows a state when both sensors are triggered during off-peak period. The cycles basically are the same as in Fig. 4 except that the time settings for green at traffic lights sited at the main roads are only 16s while narrow roads are 8s.

The timing simulation waveform illustrates in Fig. 6 differs from those in Fig. 5 in the sense that the cycle for

narrow roads are being skipped due to the reason that both sensors are not detecting or observing any vehicle.

Fig. 7 demonstrates a situation when only Sensor 1 is set off. It can be seen in the third cycle, it commences with T3 and T6 turn green for 8s. Subsequently, T3 will turn to amber for 4s and finally to red for 2s whilst T6 remain green all the time. Afterwards, the first cycle will start off again with the T1 turning green (during this time T6 remain green).

Even though with only one sensor is triggered, simulation waveform shown in Fig. 8 is dissimilar from waveform in Fig. 7. It can be seen that after the completion of the first and second cycles, since only Sensor 2 is activated, traffic light corresponding to this sensor, T5 will be green together with T2 for 8s. Both will next turn to amber for 4s and followed by red for 2s. The cycle will then continue with the first cycle where T1 and T6 turning green.

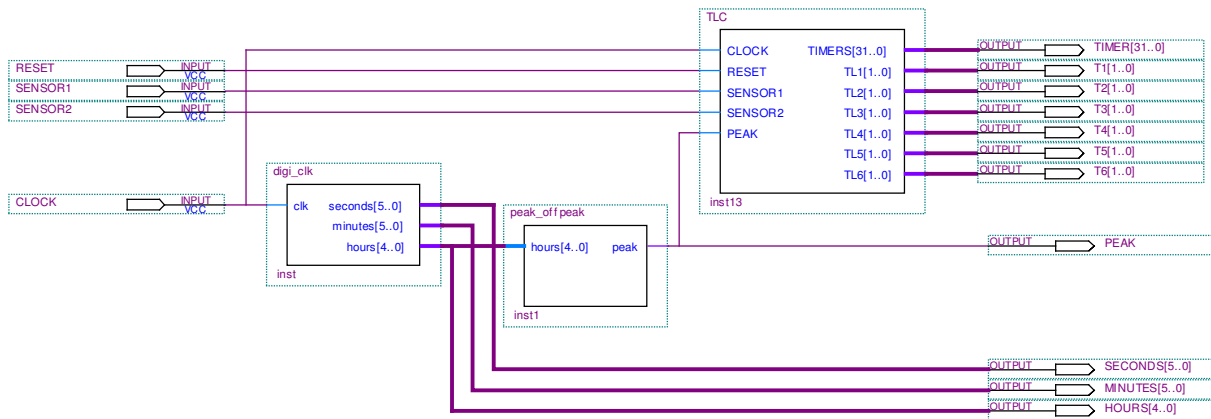


Figure 3. VHDL Model of the Controller

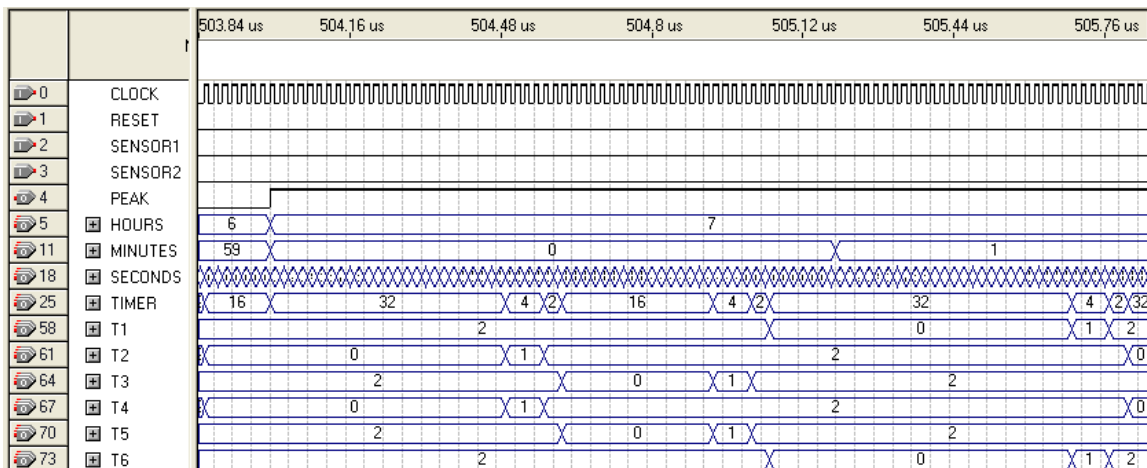


Figure 4. TLC outputs during peak hour

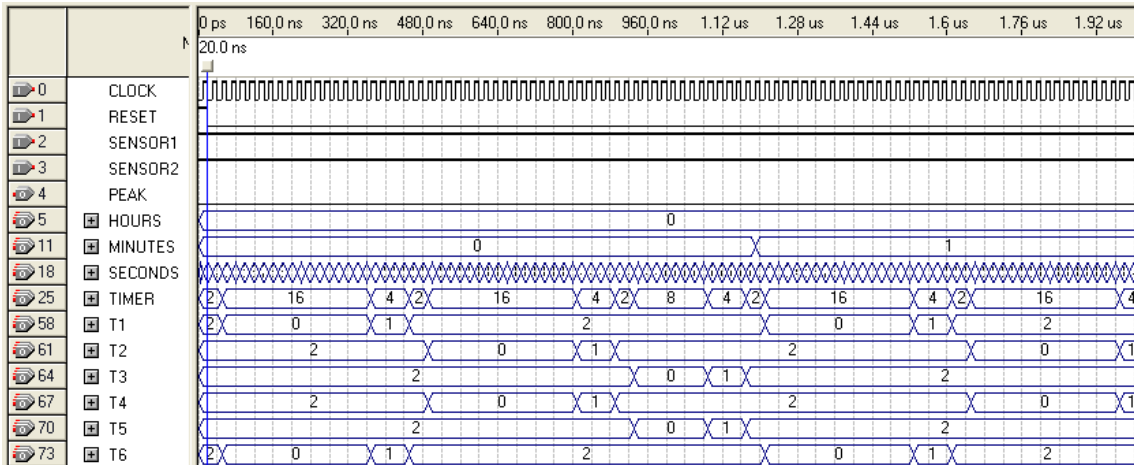


Figure 5. TLC outputs during off – peak hour with both sensors are “ON”

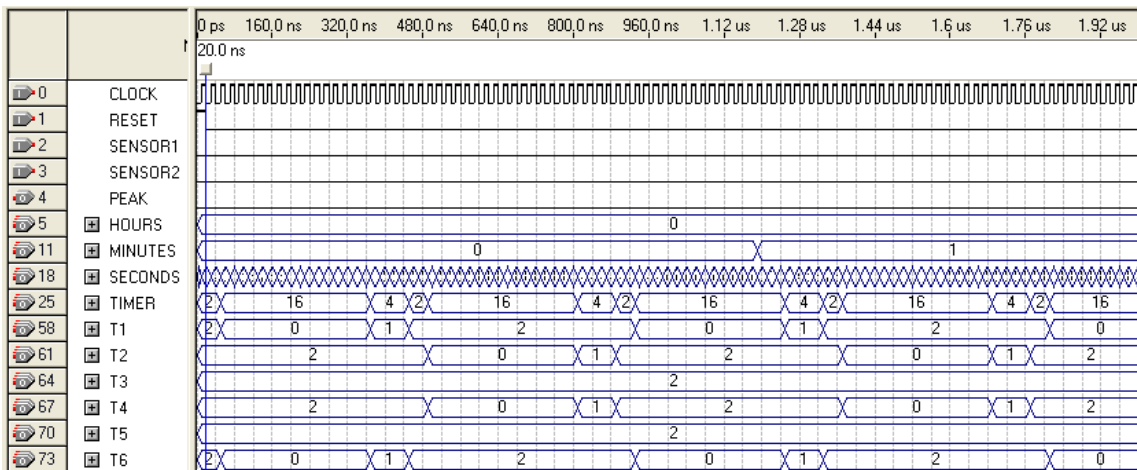


Figure 6. TLC outputs during off – peak hour with both sensors are “OFF”

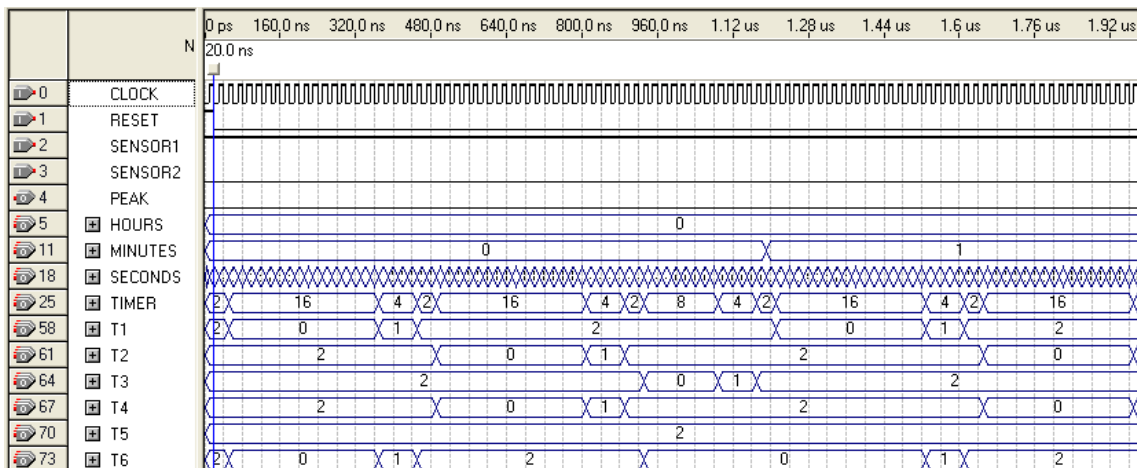


Figure 7. TLC outputs during off – peak hour with only sensor 1 is “ON”

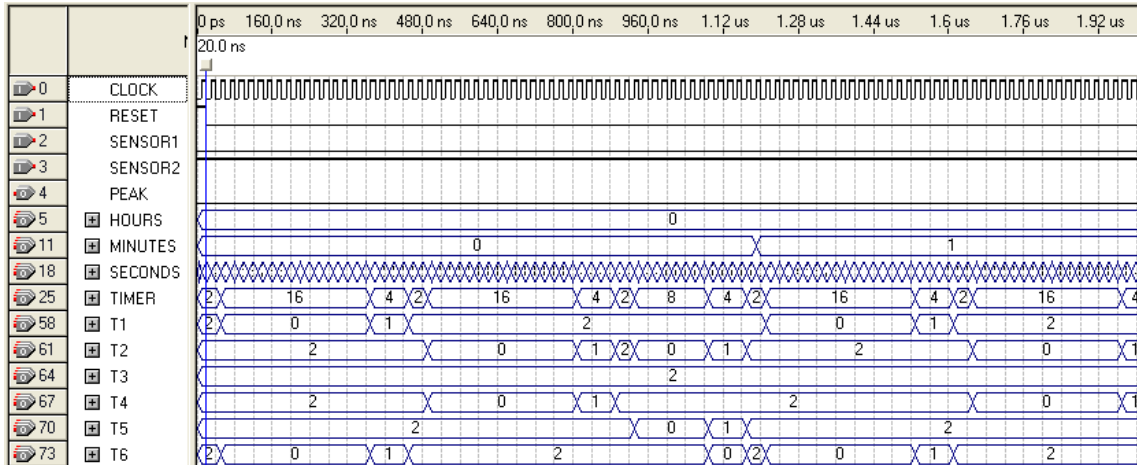


Figure 8. TLC outputs during off – peak hour with only sensor 2 is “ON”

The implementation of the TLC has successfully executed using Altera FLEX10K chip. From the observed result of the simulation, the design has reached the optimum utilization of the traffic during off-peak hour, mainly by reducing the waiting time of the driver during off-peak as well as when the sensors do not pick up any presence of car at narrow roads.

IV. CONCLUSIONS

An FPGA design of TLC with six traffic lights has been simulated using Quartus II, implemented and tested using ALTERA FLEX10K chip. One of the advantages of this design over the existing method is the waiting time of driver during off-peak hour has been reduced, means that the normal design cycle (using fixed-time technique) has been reduced notably, thus ameliorate reliability and flexibility of the TLC.

For future works, the TLC design will include pedestrian crossing lights with the intention that the reliability of the design can be much enhanced. Lastly, a comprehensive and an exceptional TLC design can be made into an embedded circuit board to control the actual traffic flow in the city’s traffic intersections.

ACKNOWLEDGMENT

This is a self-funded work and the authors wish to thank Universiti Malaysia Sarawak for supporting the dissemination of this research.

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