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Markov Chain Modeling for Router Hotspots on Network-On-Chip

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***Abstract*—A Network-on-Chip (NoC) is a current paradigm in complicated System-on-Chip (SoC) designs that renders competent on-chip communication architecture. It proposes scalable communication to SoC and grants decoupling of communication and computation. In NoC, design space exploration is vital merited to trade-offs among latency, area, and power consumption. Therefore, analytic modeling is crucial step for early NoC design. This paper delivers a top-down approach router model, and employs this model for mesh NoC performance analysis quantified in terms of throughput, average of queue size, efficiency, loss and waiting time. As a case study, the advised model is applied to map a $MPEG4$ video core to a 4×4 mesh NoC with deterministic routing to evaluate the overall NoC quality of service (QoS). The model is utilized as well to acquaints how much occupancy of average queue size for each router that reduces resources (hardware) area and cost. The accuracy of our approach and its practical use is illustrated through extensive simulation results.**

***Keywords*—**Markov chain,Network-on-Chip,router hotspots

I. Introduction

Network-on-chip (NoC) has been proposed [1] to replace system bus as the main on-chip communication technique. Owing to the breakup of computation and communication, NoC could be designed on an individual basis from the computational entities termed intellectual properties (IPs) [2]. Thus, analysis and optimization of NoC performance in terms of delay, latency, and loss are demanded. Quality-of-Service (QoS) for NoC defines the degree of commitment for packet delivery among IPs. Such a commitment can be the correctness and completion of the transaction, and bounds on the performance [3]. Researchers addressed the NoC router modeling from various lenses [9]–[12]. The work in [12] suggested a delay model for a variable pipelined wormhole router with fixed time cycle to address Lopez's model problem. Nevertheless, these models cannot be implemented for router designs that employ both clock edges and moreover they did not examine the affect of varying router design parameters on its delay. The router queue modeling also still need to be directed because it is vital to acquire an approximation of the optimal queue size that matches the target traffic characteristics at the higher levels of abstraction. The challenges for NoC research are on assisting early design space exploration for NoC-based SoC. Good traffic and NoC performance estimation could significantly shed some light to probable NoC design aspects. This work considers router model that forecasts an NoC router performance. This paper presents a performance analysis of mesh NoC in terms of throughput (Th), average queue size (Qa), loss (L), and waiting time (W). A discrete-time Markov model of mesh NoC topology is obtained, which helps decision-making in terms of switching techniques, buffer sizes, and router types. Moreover, this also helps to identify router and link hotspots for better packet routing. The rest of the paper is organized as follows. In Section II and Section III, we discuss related works on modeling NoC infrastructure. Section and V proposes the Markov chain modeling of NoC. Section IV discusses analysis from MPEG4 cores. Section IV corresponds to an experimental results of our method by a case study. Finally, Section VII conclude this paper.

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II. Related Works

System bus is a circuit-switching, connection-oriented on-chip communication backbone. Meanwhile, NoC practices packet-switching, which segments the message into a sequence of packets [4] transmitted to a shared network. On-chip networks share the similar features in topology, switching, routing, and flow control with local area network (LAN) [13]. Moreover, NoC has to render high and predictable performance [5] with small area overhead and low power consumption. An essential problem in NoC is the router design, since it significantly impacts the network performance as well as power consumption. An effective router design is specified by its switching technique, flow control type, queue size, arbiter design, routing strategy. Chien et al. [14] proposed a delay model for wormhole and virtual channel routers. Even so, this model was designed for $0.8 - micron$ CMOS and can not be implemented to pipelined architectures. Lopez et al. [16] advised an extension to Chiens model for pipelined routers. However, Lopezs model presumes that the time duration of the clock cycle counts on the router latency, which is impractical assumption. Peh et al. [12] suggested a delay model for a variable pipelined wormhole router with fixed time cycle to address Lopezs model problem. Yet, these models can not be applied for router designs that apply both clock edges. The router queue modeling still necessitate to be covered as it is supercritical to acquire an estimation of the optimum queue size that matches the target traffic characteristics at higher levels of abstraction. Due to limited buffers [6] and link bandwidth, packets might be barred due to contention [7]. Buffer sizing has a direct association with bounds in bandwidth, delay and

jitter [8].

III. NoC Structure

This section provides background on NoC architectural issues. These issues include network topology, router structure, switching techniques and routing algorithms.

A. Topology

This architecture is based on an $m \times n$ mesh network whereas every router, except those at the edges, is connected to 4 neighbouring routers and 1 IP through communication channels [15]. This topology grants integration of large number of IP cores in a regular-shape structure. A channel consists of two unidirectional links between two routers or between a router and a resource. Fig. 1 shows a 4×4 mesh NoC with 16 functional IP blocks. Every router has 5 ports, 1 connected to the local resource and the others connected to the closest neighbouring routers.

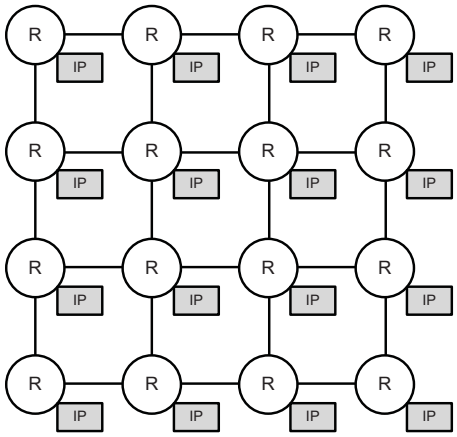

Fig. 1. 4×4 Mesh Topology

B. Router Structure

Router operates at the network layer similar to computer network. A router uses packet headers and a forwarding table to determine the best route a packet should go among the networks. An NoC router has three main architectural components which are input/output (IO) ports, queues, and switch fabric (SF). The SF establishes the required paths between pairs of IO ports according to a certain routing mechanism such as round-robin scheduler, weighted round-robin scheduler, and max-min fairness scheduling [18].

Fig. 2 shows an input-queuing router. Each input port has a dedicated first-in first-out (FIFO) queue for storing incoming packets. In one time step, an input queue must be able to support one write and one read operations. Assuming an $n \times n$ router, the switch fabric must connect n input ports to n output ports [18]. The main advantage of an input queuing router is the low memory speed requirement, distributed traffic management at each input port, and also distributed table

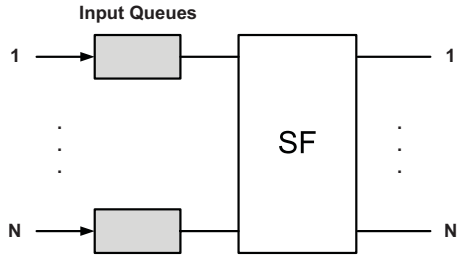

Fig. 2. Input-queuing router

lookup at each input port. It is supports packets broadcast and multicast without the need to duplicate the packet.

C. Switching Techniques

As an alternative to circuit switching, a message can be partitioned and transmitted as fixed-length packets by packet switching. Packets are individually routed from source to destination. A packet is stored at each intermediate node then forwarded to the next node. Packet switching is good for short and frequent messages [19]. Traditional designs borrowed from LAN result in limiting performance bottleneck. Some new switching techniques, such as virtual cut-through (VCT) and wormhole switching techniques have been proposed to improve NoC performance [19]. To construct small router that resides in an on-chip component, wormhole switching is usually used [19]. This work assumes wormhole switching because this switching expects less queue capacity and allows low-latency communication.

D. Routing

Routing algorithms are used to specify the path from source to destination for each message. They can be implemented in two ways which are either deterministic or adaptive [19]. Deterministic routing protocol chooses the path for a message only by its source and destination. All packets with the same source and destination pair will follow one single path. The packet will be delayed if any channel along this path is loaded with heavy traffic, and if a channel along this path is faulty, the packet cannot be delivered. Thus, the deterministic routing protocols suffer from poor use of bandwidth, and blocking even when alternative paths are available. Adaptive routing protocols are proposed to make more efficient use of bandwidth and to improve fault tolerance of interconnection network. In order to achieve this, adaptive routing protocols provide alternative paths for communicating nodes. Thus, it could overcome the congested areas in the network. Several adaptive routing algorithms have been proposed, showing that message blocking can be considerably reduced, thus strongly improving throughput [16].

IV. Markov Chain Approach for Network-on-Chip Modeling

There are several approaches to modeling NoC. Several works [1]–[4] focus on stochastic models. This project could be conceptualized from top-level system design. It starts with the highest level of NoC view, and works its way down to every single component in NoC block diagram.

A. Modeling Abstractions

An NoC-based SoC system is composed from an NoC topology and IP blocks.

1) NoC-level Abstraction: Fig. 3 shows a SoC system which composed of NoC and IP blocks. The NoC provides decoupling computation (IP) and communication parts. This allows for IPs and interconnects to be designed independently.

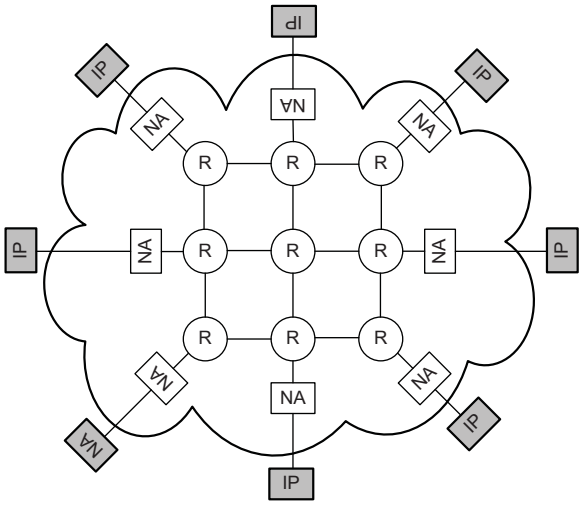

Fig. 3. NoC-level Modeling Abstraction

2) Topology-level Abstraction: Fig. 1 shows the top level view of a 4 mesh topology for NoC modeling. Two elements on NoC are router and network adapter (NA). The NA is used as interfaces between IP blocks and NoC. Meanwhile, the function of the router is to transport data from one NA to another.

3) Router-level Abstraction: $m \times n$ mesh topology is used, whereas each router has the maximum 5 IO ports. 4 ports are connected with others routers and 1 port to the IP.

B. Performance Metrics

The NoC performance is analysed in terms of several metrics which are throughput, average queue size, and packet waiting time.

1) Throughput in units of packets per time step which describes how many end-to-end packet transfer
2) Average Queue size is queue occupancy queue size which is measured in units of packets.
3) Waiting time is the latency in terms of time step, where time step is define as the time to transfer a packet on a local link
4) Average lost traffic is measured in units of packets per time step.

C. $M/M/1/B$ Queue Modeling

This section presents an analytical model for input-queuing router. Each queue is considered as a FIFO queue. The model has simple close-form calculations and produces the performance of the queue. A simple $M/M/1/B$ queue is used in this model. This model provides a discrete-time Markov chain [18] analysis of queue where the time step is taken equal to the time required to transmit a packet. Poisson distribution traffic arrival process and the exponential distributed service time is assumed. For each queue model, one server queue with B finite buffer size are assumed.

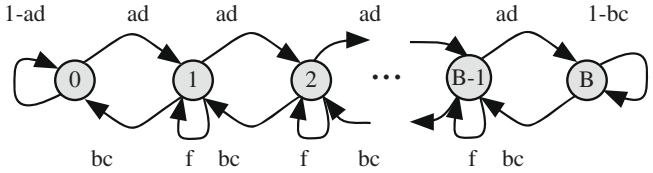

Fig. 4. State transition diagram for an M/M/1/B queue.

Fig. 4 shows, the state transition diagram for the discrete-time Markov chain $M/M/1/B$ queue. A homogeneous Markov Chain is considered since packet arrivals and departures are independent of the time index value [18]. From state transition diagram in Fig. 4, the state transition matrix $\mathbf{P}$ [18] is defined as

$$\mathbf{P} = \begin{bmatrix} 1-a & bc & \cdots & 0 & 0 \\ a & f & \cdots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & f & bc \\ 0 & 0 & \cdots & ad & 1-bc \end{bmatrix} \tag{1}$$

The difference equations for the state probability vector [18] can be expressed as

$$\mathbf{s} \;=\; [\; s_0 \quad s_1 \quad \cdots \quad s_{B-1} \quad s_B \;]^t \tag{2}$$

where s_i is the probability that the queue contains i packets, and is given as:

$$s_i = \rho^i d^{i-1} s_0 \qquad \text{for } 1 \le i \le B \tag{3}$$

with ρ is defined as:

$$\rho \;=\; \frac{a}{bc} \tag{4}$$

Satisfying the condition $\sum_{i=0}^{B} s_i = 1$ from [18] gives:

$$s_i = \frac{(1-\rho d)\rho^i d^{max(0,i-1)}}{1+\rho(c-\rho^B d^B)} \qquad \text{for } 0 \le i \le B \tag{5}$$

TABLE I
GENERAL ROUTER AND NOC PERFORMACE EQUATIONS. q_j REFERS TO j-TH QUEUE IN ROUTER r_i.

Variables	router r_i	NoC
Throughput Th	$\frac{1}{\lvert N\rvert}\sum_{j=1}^{N} Th_{q_j}$	$\frac{1}{\lvert r_{total}\rvert}\sum_{i=1}^{N} Th_{r_i}$
Queue occupancy Qa	$\frac{1}{\lvert N\rvert}\sum_{j=1}^{N} Th_{q_j}$	$\frac{1}{\lvert r_{total}\rvert}\sum_{i=1}^{N} Qa_{r_i}$
Loss probability L	$\frac{1}{\lvert N\rvert}\sum_{j=1}^{N} L_{q_j}$	$\frac{1}{\lvert r_{total}\rvert}\sum_{i=1}^{N} L_{r_i}$
Waiting time W	$\frac{1}{\lvert N\rvert}\sum_{j=1}^{N} W_{q_j}$	$\frac{1}{\lvert r_{total}\rvert}\sum_{i=1}^{N} W_{r_i}$

From Little's result [18], the average queuing delay ϕ is given by:

$$\phi = \frac{Qa}{Th} \tag{6}$$

where Qa is the average queue occupancy and Th is the average queue throughput in packet per time step. The throughput, Th, is defined as the probability that the queue is served while it is not empty, and is given by:

$$Th = c\,(1 - s_0) \tag{7}$$

The average queue occupancy Q is given by:

$$\begin{aligned} Q &= \sum_{i=0}^{B} i\ s_i \\ &= \frac{1-\rho d}{1+\rho(c-\rho^B d^B)} \sum_{i=1}^{B} i\rho^i d^{i-1} \end{aligned} \tag{8}$$

A packet is said to be lost when the queue is full when the a packet arrives and none is serviced. Thus, the loss probability, L, is given by:

$$L = s_B\ a\ d \tag{9}$$

D. Router and NoC Modeling

This section discusses the generation of general router performance. General router equation performance is generated from average of all queues in a router. There are the equations of throughput, efficiency, average queue size, loss, and wait time for a router r_i. The overall performance in term of throughput, average queue size, wait time, and loss are obtained by averaging all 16 routers in a 4×4 mesh NoC. The general NoC performance is given in Table I.

V. ANALYSIS OF MPEG-4 CORES

Fig. 5 shows a proposed methodology in a case study for video application (MPEG4 core) to analyse the performance of mesh NoC from various metrics which are throughput,average queue size, loss, and waiting time.

A. MPEG4 SoC Traffic Distribution Graph

As shown in Fig. 5, a traffic distribution graph (TDG) for the typical video applications (MPEG4 core) is considered the main design input. The numbers written on the arrows are the average number of packets transmitted and the numbers written on the circles represent the IPs number. From a given TDG, traffic distribution matrix (λ) is generated. The generated matrix is organized such that λ_{ij} represents the number of packets transmitted from a node IP_j to IP_i.

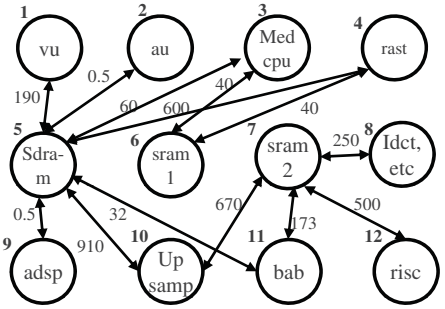

Fig. 5. MPEG4 core [20]

$$\lambda = \begin{bmatrix} 0 & 0 & 0 & 0 & 190 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.5 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 60 & 40 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 600 & 40 & 0 & 0 & 0 & 0 & 0 & 0 \\ 190 & 0.5 & 60 & 600 & 0 & 0 & 0 & 0 & 0.5 & 910 & 32 & 0 \\ 0 & 0 & 40 & 40 & 190 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 250 & 0 & 670 & 173 & 500 \\ 0 & 0 & 0 & 0 & 0 & 0 & 250 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0.5 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 910 & 0 & 670 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 32 & 0 & 173 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 500 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{10}$$

B. IP Mapping and Routing

IPs mapping and routing for the MPEG4 cores through the routers in 4×4 Mesh NoC with deterministic routing is shown in Fig. 6. All communication between IP blocks with same source and destination always go through same path of router through shortest path. Connectivity matrix is then formed through IPs routing. A packet with same source and destination go through the specific routing path that had been determined. The total no of hops used is 35 as shown in Table II.

C. Routing Matrix

From the connectivity matrix, the input port is identified for communicating with output ports of each router. Then, remove those set of input to output connections that are not used for routing paths. This reduce resources area in the NoC. Equation 11 shows the example of routing table and routing matrix for router number 10 (R_{10}) in the 4×4 mesh NoC.

$$rm_{R10} = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 \\ 1 & 0 & 0 & 1 & 0 \\ 1 & 0 & 1 & 0 & 1 \end{bmatrix} \tag{11}$$

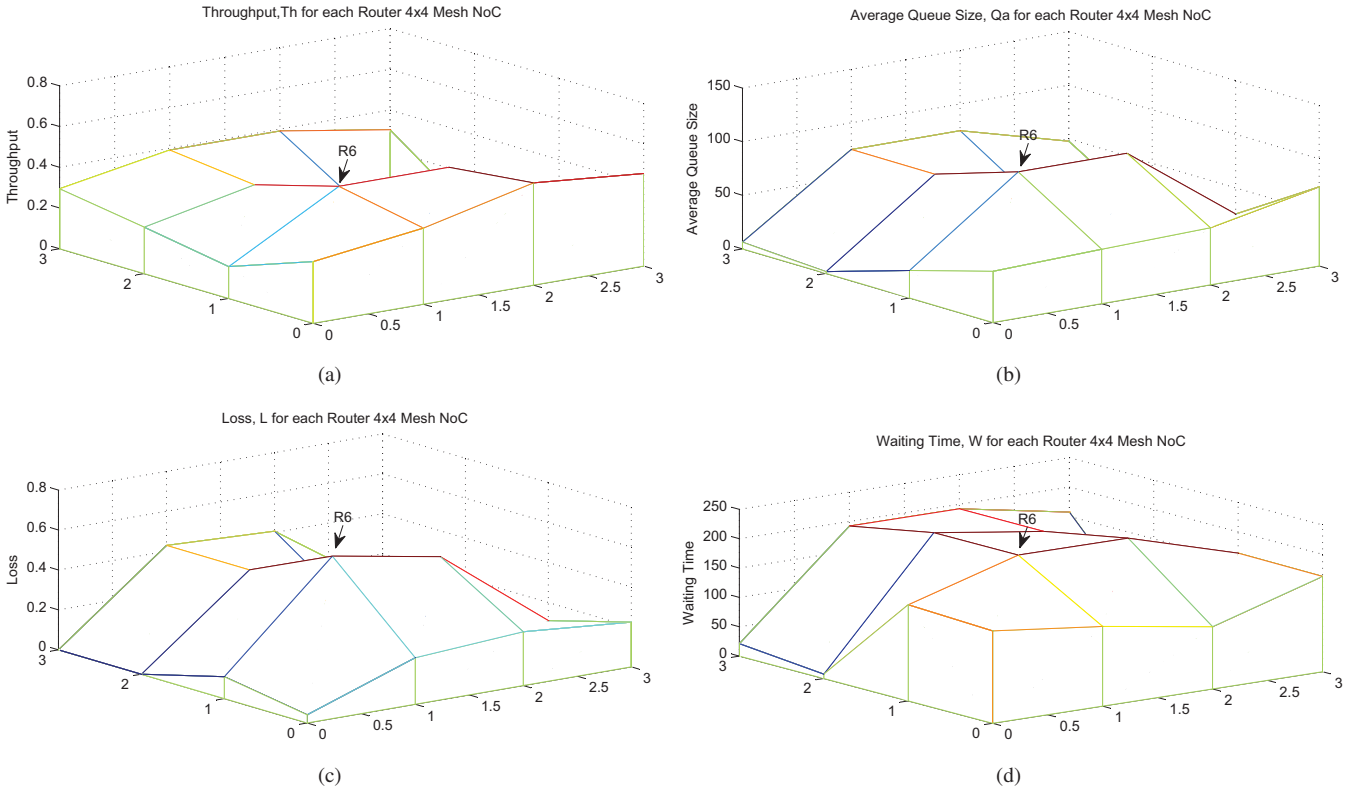

Fig. 7. The average performance for all 16 routers in the 4×4 mesh NoC (a) Throughput, (b) Average queue size, (c) Wait time, and (d) Loss.

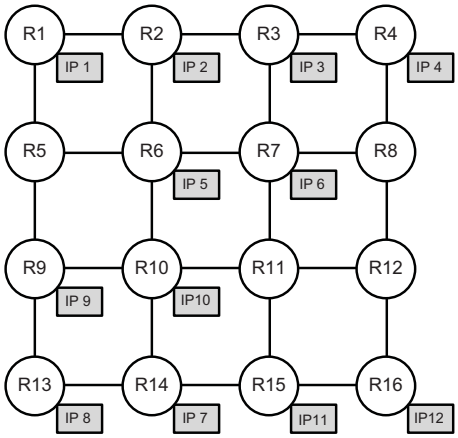

Fig. 6. MPEG4 core IPs is mapped in 4x4 mesh NoC

TABLE II
MPEG4 CONNECTIVITY MATRIX

Communicating IPs	Routing path	No of hops
$IP_1 \leftrightarrow IP_5$	$R_1 \leftrightarrow R_5 \leftrightarrow R_6$	3
$IP_2 \leftrightarrow IP_5$	$R_2 \leftrightarrow R_6$	2
$IP_3 \leftrightarrow IP_5$	$R_3 \leftrightarrow R_7 \leftrightarrow R_6$	3
$IP_3 \leftrightarrow IP_6$	$R_3 \leftrightarrow R_7$	2
$IP_4 \leftrightarrow IP_5$	$R_4 \leftrightarrow R_3 \leftrightarrow R_2 \leftrightarrow R_6$	4
$IP_4 \leftrightarrow IP_6$	$R_4 \leftrightarrow R_8 \leftrightarrow R_7$	3
$IP_5 \leftrightarrow IP_5$	$R_6 \leftrightarrow R_{10} \leftrightarrow R_9$	3
$IP_5 \leftrightarrow IP_{10}$	$R_6 \leftrightarrow R_{10}$	2
$IP_5 \leftrightarrow IP_{11}$	$R_6 \leftrightarrow R_7 \leftrightarrow R_{11} \leftrightarrow R_{15}$	4
$IP_7 \leftrightarrow IP_8$	$R_{14} \leftrightarrow R_{13}$	2
$IP_7 \leftrightarrow IP_{10}$	$R_{14} \leftrightarrow R_{10}$	2
$IP_7 \leftrightarrow IP_{11}$	$R_{14} \leftrightarrow R_{15}$	2
$IP_7 \leftrightarrow IP_{12}$	$R_{14} \leftrightarrow R_{15} \leftrightarrow R_{16}$	3

VI. EXPERIMENTAL RESULTS

To verify the performance analysis, overall mesh NoC performance in term of throughput, average queue size, loss, and waiting time are performed. Initial mapping of 12 IPs MPEG4 core in 4×4 mesh NoC modeling is made through the shortest path XY deterministic routing given in Table II and Fig. 6. Simulation was performed and the router loading performance analysis for all 16 routers is shown in Fig. 7. Fig. 7 shows that all 16 routers give different performance in mesh NoC due to the router loading and IPs traffic. Fig. 8 clarifies that router six $(R6)$ is determined as a router hotspot that gives the worst performance - 100% packet lost and waiting time. As can be seen from Fig. 6, R6 is connected to IP5 that has a highest traffic rate. Therefore, all five queues of $R6$ have been mostly occupied with packets. The average of throughput for this mesh NoC is 54%. The $R9$ that is attached with $IP9$ gives a best performance with 4% loss, and only 4% waiting time. Congestion could be characterized by decreased throughput, increased loss, and increased wait

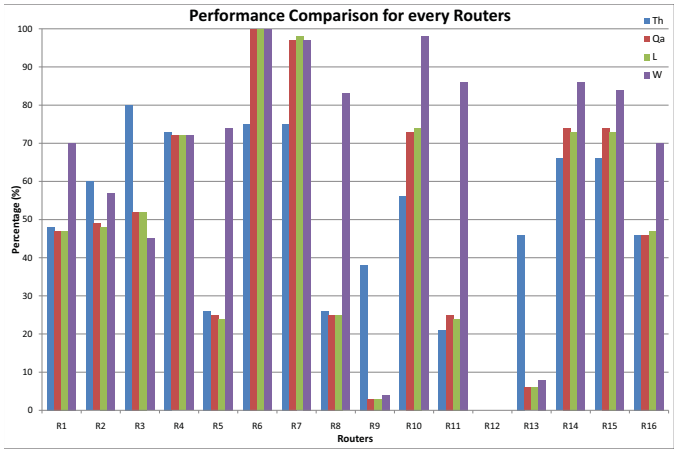

Fig. 8. Hotspot

time. The main reason to identify router hotspots in NoC is to improve the overall performance of NoC. Hence, IPs of router hotspot could be rerouted possibly until the best performance could be achieved. From this router loading analysis, an early idea of mapping IPs that have different traffic rate could be set up for each router. The occupancy of average queue size also could be obtained with specific routes. Therefore, the resource hardware area and cost could be reduced in the NoC topology.

VII. Conclusions and Future Works

This paper presented a Markov chain model for identifying router loading and hotspots. An analytical model for 4×4 mesh NoC with a video application MEPG4 cores is presented. NoC performance metrics such as throughput, waiting time, queue size, efficiency, and loss could be easily identified from the model output. The complete success of the models described here cannot yet be claimed without further research investigation. There are many interesting possibilities for future research here and the most important of these are, extending this modeling approach with other NoC topologies, router types, and queue models. Another challenging problem is to improve the model to automatically place each IP to the most optimum NoC tile. Finally is to prototype the NoC.

VIII. Acknowledgement

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