TOPOLOGICAL DESIGN EXPLORATION FOR 10×10 MESH WIRELESS NETWORK-ON-CHIP

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Bachelor of Engineering (Hons)

Electrical and Electronics Engineering

2022

A dissertation submitted in partial fulfilment
of the requirement for the degree of

Faculty of Engineering

Universiti Malaysia Sarawak

2022

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ACKNOWLEDGEMENT

First of all, a lot of respect and thanks to my honorable supervisor, Mr Asrani Lit who is there with me upon completing the Final Year Project 1 and 2. Not to forget for the guidance and encouragement that been given during completing this project from the Final Year Project 1 and 2. It been a pleasure to work with Mr Asrani as my supervisor. Also, thanks to the helpful advices and hard work from all examiner that evaluate my presentation and report of this project. It is very much appreciated. A special gratitude also to Dr Dayang Nur Salmi Dharmiza Awang Salleh as the coordinator for this subject of Final Year Project 2. Next, an appreciation dedicated to all friends who are with me directly or indirectly in completing this precious project even though there were many challenges occur during the process. Last but not least, a big love and thanks to my family that help and provide me need in finishing my final year project. There are so many contributions that it is impossible to write them all down on paper. Once again, thanks to all that involve in this project directly or indirectly.

ABSTRACT

Wireless Network on Chip is an innovative technique to resolving latency and power consumption limitations in Network-on-Chip (NoC). This project targets to improve the performance of the Wireless Network on Chip (WiNoC) on different radio hub location for 10×10 MESH topology. As WiNoC has gotten bigger as a communication technology, it has encountered issues with topological performance that must be addressed. The system with high latency will affect the network throughput. Thus, the power consumption by system might get higher due to many workloads. The power consumption model and the system interference model have been offered as methods for achieving the desired topology generation. By utilizing the cycle accurate on chip simulator (Noxim), the experimental simulation compares three topologies with different placements for the radio hub in order to assess how well each one performs in terms of latency, network throughput, and energy consumption. By this experiment, the best topology is the 4-hub topology (WiNoC).

ABSTRAK

Rangkaian Tanpa Wayar pada Cip adalah teknik inovatif untuk menyelesaikan kependaman dan had penggunaan kuasa dalam Rangkaian pada Cip (NoC). Projek ini menyasarkan untuk meningkatkan prestasi Rangkaian Tanpa Wayar pada Cip (WiNoC) pada lokasi hab radio yang berbeza untuk topologi 10×10 MESH. Oleh kerana WiNoC telah menjadi lebih besar sebagai teknologi komunikasi, ia telah menghadapi masalah dengan prestasi topologi yang mesti ditangani. Sistem dengan kependaman tinggi akan menjejaskan throughput rangkaian. Oleh itu, penggunaan kuasa oleh sistem mungkin menjadi lebih tinggi kerana banyak beban kerja. Model penggunaan kuasa dan model gangguan sistem telah ditawarkan sebagai kaedah untuk mencapai penjanaan topologi yang dikehendaki. Dengan menggunakan kitaran yang tepat pada simulator cip (Noxim), simulasi eksperimen membandingkan tiga topologi dengan penempatan yang berbeza untuk hab radio untuk menilai sejauh mana prestasi masing-masing dari segi kependaman, throughput rangkaian, dan penggunaan tenaga. Dengan percubaan ini, topologi terbaik adalah topologi 4-hub (WiNoC).

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LIST OF ABBREVIATIONS

2D Mesh	:	2-Dimensional Mesh
CMOS	:	Complementary metal-oxide semiconductor
FYP	:	Final Year Project
HCCT	:	Heterogenous and Hybrid Clustered
Linux OS	:	Linux Operating System
Mac OS	:	Mac Operating System
MCR	:	Mesh Connected Ring
NoC	:	Network On Chip
OUC	:	Octagon for Ubiquitous Computing
TCR	:	Torus Connected Ring
WiNoC	:	Wireless Network on Chip
NIRGAM	:	Interconnect Routing and Application Modelling

CHAPTER 1

INTRODUCTION

1.1 Overview

This chapter will be an overview of introduction about studied project or topic which involves the project background, problem statements, objectives of the project, scope of study as well as the project outline.

1.2 Problem Statement

Topology is among the key determinant factors that influence the performance of WiNoC as wireless connectivity is a viable solution that provides high bandwidth and low latency while increasing energy efficiency [7]. High power efficiency for long one-hop communications, reduced complexity compared to systems using waveguides or cables, and compatibility with wireless complementary metal oxide semiconductor (CMOS) technology designs are all benefits of wireless connectivity. is. A wireless connection allows you to send data in a single hop over the chip with minimal power consumption. This when design of topologies plays its role.

Next, the selection of topology plays an important role in determining the overall performance of WiNoC. As we all known, different topology has its own pros and cons. As example, how to improve the efficiency of the system and make the system faster to transmit the data so receiver can receive the data without a big delay. Then, system not running at the highest performance although the topology use is suitable according to requirement. Unfortunately, many people face lagging when transfer data although they using suitable topology according to their requirement. This delay or drag of time affect their work in daily lives. For example, large size of file been transfer but it took half hour to receive which mean whole team will be drag to this problem.

1.3 Objectives

The overall idea of this research is to learn about the workings and structures of Network-on-Chip (NoC) and Wireless Network-on-Chip devices (WiNoC). Discovering how the cycle accurate on chip simulator (NOXIM) operates is also important.

The following are the project's main aims:

1. To investigate the impact of various topologies in term of number of radio hub for 10×10 MESH WiNoC
2. To make a comparative analysis of the impact of radio hub placement as numerous topological structure

1.4 Scope of study

For this final year project, MESH topology been used and the devices set was 10 by 10 arrangement. Then, the topology been set with three different conditions. Which are first MESH topology been added with 4 hub, second topology added 8 hub and last topology has 12 hubs. By this difference, we can observe the latency, the delay, throughput and energy in the system.

End-to-end delays and network delays were the two categories or sorts of delays. What was the difference between network and end-to-end delay? For one-way communication, end-to-end delay is the time it takes for a packet to transit from transmitter to the receiver or from one point towards another [8]. Network latency, on either way, is focused on network delay measured in either one or both ways. The time it takes to send a packet from the transmitter to the receiver plus the time it takes to send the packet right to the original is used to calculate bidirectional network delay. The system's energy demand is next.

For increased versatility, on-chip communication technology integrates a multi-core design with numerous computer processing centres on a single silicon chip integrated circuit (IC). Despite the majority of the benefits of the traditional network-on-chip (NoC) architecture, an increase in the number of NoC processing cores resulted in higher latency and energy consumption in the system design because of multiple-hop, long-distance communication. In order to solve the problems of excessive latency, energy dissipation,

and throughput in NoC, wireless network-on-chip (WiNoC) technology was developed. On top of a typical NoC, it is a wireless framework. It has a large bandwidth, optimal energy, and low latency since it can deliver data to far-off core processors with just one hop and little energy consumption.

The WiNoC structure is broken into numerous smaller knots of adjacent cores, or subnets, that are used to organise it. It has fewer cores than conventional processors, which gives system architecture more freedom. The cores were wirelessly linked to every subnet's node in the network as well as directly attached to a central node. On the other hand, virtual channel flow control offers a different link to boost network effectiveness. Virtual channel flow blocking by using several virtual channels in place of a physical channel. The virtual channel idea was developed for the demonstration of a deadlock-free link in wormhole switching networks.

1.5 Chapter outline

For this Final Year Project 1, there will be three chapters. The topics that are elaborate in this Chapter 1 is including chapter overview, the background of the project, problem statement, objectives of the project, scope of study and chapter summary. This chapter mainly to introduce the vision of project.

Next, in Chapter 2 consists of a few topics which including the overview of NOXIM simulator, radio hub and related article that related with the project. The goal of this chapter is therefore to explore, compare, and examine the theories and approaches associated with this project. In this study, all of the papers mentioned in Chapter 2 will be used as references and comparisons.

Lastly, in Chapter 3 start with overview and some brief elaboration of the overall project flow. Then, elaborate more about how to implement the topologies into NOXIM simulator as proposed work.

For Final Year Project 2, it will cover Chapter 4 and Chapter 5. In Chapter 4, will go into more detail about the analysis and discussion of the results. This chapter also covers the issue that arose during the project's completion. The information is gathered, and the simulation's outcomes will be seen. The outcome is compared to published reference materials like technical papers.

Then, Chapter 5 is about the results of this project and suggestions for the future.

We'll go into more detail about the data that has been collected and the project goals that have also been met. Each suggestion will be described as a future reference for the emotion recognition task.

1.6 Chapter Summary

In conclusion, this chapter was brainstorming the idea of the project. Then, come out with some aim to achieve at the end of the project. With a good structure in Chapter 1, Chapter 2 and Chapter3, Final Year Project 1 will set a good outcome for Final Year Project 2. As both of this are related and affect each other's. The result gained will be determine on how good the parameter been set and design during first three chapter. Plus, identify why the project has been done at the first place. Lastly, briefly introduce the concept of the project.

Chapter 2

LITERATURE REVIEW

2.1 Overview

The literature review for the research paper will be presented and elaborated in this chapter. The research works from previous projects will be displayed in the linked study. In addition, the research gap will be explained. Finally, a summary of the entire literature reviews will be provided.

The three fundamental elements that Network-on-Chip (NoC) parts are comprised of are routers, connectors, and network interfaces. Each of these parts serves a particular purpose, such as routers, which transfer data in packet form until it reaches its destination in accordance with a predetermined routing protocol, links in the form of wires, which link routers to other routers, and the network interface, which links the router to each core on the chip. The distance between nodes increases as the network gets bigger. Due to increasing levels of integration and the number of cores per device, sustainable, somewhat increased on-chip networking has been a significant topic of research. A sort of technology known as Network-on-Chip (NoC) was developed in order to improve Network-on-Chip performance and address the problem of excessive communication delay between cores in multi-core architecture (NoC). Network-on-Chip (NoC) has been used to create accelerators and specialised processing units in a variety of applications, including reconfigurable computing, cloud computing, the internet of things, networking, and storage. This is because NoC may benefit from tremendous parallelism. Since the introduction of multi-core chip processors in recent years, the on-chip network has grown to represent a sizeable portion of the chip's overall power budget.

Messages are often sent through the Wireless Network-on-Chip (WiNoC), which increases the need for bandwidth, the lag time in the communication system, and the power consumption. In order to solve the issue of high communication latency between cores in a multicore design, the Network-on-Chip (NoC) architecture was developed. The needs in this field cannot be entirely satisfied by improving the properties of metal links,

hence new interconnections must be proposed. Wave wireless interconnects, crossbar on chip interconnects, concentrated-sparse mesh, and other interconnects have all been suggested to alleviate latency and power issues [16]. Although these methods can reduce latency and power usage, they have production and design flaws. When it comes to data transfers involving long-distance transmission and network connection delay, Wireless Network-on-Chip (WiNoC) might be viewed as a type of Network-on-Chip (NoC).

Time delay, power consumption, and throughput are the three main metrics used to assess a NoC system's performance. Latency is the amount of time (measured in clock cycles) that elapses between the source node injecting a message header into the network and the destination node receiving the message tail. Network latency, also referred to as "lag," describes delays in communication via a network. In networking, latency is the length of time it takes for a packet of data to be gathered, transported, processed by various devices, then received at its destination and decoded. A high-latency network (unwanted) has longer delayed while a low-latency network (preferred) has much smaller delays (not so desirable). Long delays in high-latency networks cause communication bottlenecks [17]. In the worst-case scenario, it's comparable to traffic trying to merge into a single lane on a four-lane highway. High latency limits transmission bandwidth and may be either temporary or permanent, depending on the cause of the delays. One of the main causes of network delay is distance, or the distance between the device making the request and the servers responding to it. Latency, throughput, and power are the three most important and fundamental performance evaluation factors in the core integration. Consistently monitoring transmission data, the congestion unit of measure assesses throughput, delay, and power under varied traffic loads. When throughput stops increasing, saturation load is examined.

Communication quality is favourably influenced by latency, bandwidth, and throughput. Although these three criteria are related, they have separate meanings. Consider data packets travelling across a conduit to better understand it. The bandwidth represents the width of the conduit. A pipe is thinner the less information that can flow back and forth across it. A communication band's width increases with the amount of data that may be transmitted through it at once. Latency [17] is the speed at which data packets inside the pipe go from the client to the server and back. Packet latency is the physical distance that data must cover in order to reach its destination through cables, networks, and other hardware. Throughput is the measure of how much data can be transferred in a

given amount of time. Throughput will be minimal as well because to the evident low latency and bandwidth. This means that even though theoretically data packets should arrive instantly, insufficient bandwidth can nonetheless result in serious congestion. The throughput will be better and the connection will be more effective if the connection has a high bandwidth and low latency.

2.2 Background of the project

A communication organisation strategy for operating modules on the same chip is known as "Network on Chip" (NoC). Electrical equipment may be installed on silicon crystals, and it tries to bring together a variety of computer cores (executive, graphics, physics, and so forth). Network-on-chip (NoC) is considered to have a very promising future for additional micro components in the area of microprocessor technology [22]. When large or outdated communication systems, like telephones, evolved, the wire connections first appeared directly and used analogue; next, matrix switches and crossbars appeared; next, signal relay switching (analogue - a modern version of NoC); and finally, digital switching with a focus on packet transmission. For instance, the TCP/IP protocol is actively being used to create the NoC equivalent for the Internet.

Network topology is the way a network is arranged, including the physical or logical description of how links and nodes are set up to relate to each other. Topology plays an essential role on how well your network will be functions. By choosing the correct topology for required system or network, it can improve performance and make it easier to detect faults, troubleshoot errors, and allocate resources more effectively across the network to ensure optimal network health.

During this pandemic, a lot of works been digitalized and it is required a good device to help or finish the works. For example, nowadays meeting been conducted via Cisco Webex or Microsoft Teams platform compare to before pandemic, which people can gather face to face without any social distancing. So, big companies that create technologies evolve according to current situation and demand from users. Most of the apps nowadays consume a lot of space and data to run it.

To overcome this problem, technologies and engineer try to create the best topologies to make the system more efficient and run faster. There a lot type of topologies that have

different advantages and disadvantages. Some of example of topologies is MESH topology, BUS topology, RING topology and STAR topology. But in this modern world, hybrid topology is more widely used due to it has more advantages than single type of topology.

2.2.1 MESH topology

As we known, MESH topology was the common or well use in network on chip. Figure 2.1 shows a mesh topology which define as a network setup where each computer and network device are interconnected with one another. Most transmissions can be distributed using this topology even if one of the connections fails. There are some advantages by using this topology such as an error or failure in the system will be easy to detect and if one of the links in the system failed it will not affect other links and the communication between other devices on the network. There is still a unique connection between the transmitter and receiver that can only be utilized by both devices, thus traffic load is not an issue. Thesecurity also secure because there is a point-to-point link in the mesh topology so unauthorized user or access is impossible. Besides, having advantages, the topology is not perfect and has its own disadvantages. For example, Scalability challenges arise as aresult of the inability to match gadgets to a wide variety of component via specialized level links [1]. Based on its definition, we can assume a lot of port network used and the usage of wired to connected the hub were many. Sometimes the arrangement of the wiredcan be complicated and consume longer time to build the system. So, to build and maintaining the system will cost a high price and has potential to reduce the system efficiency.

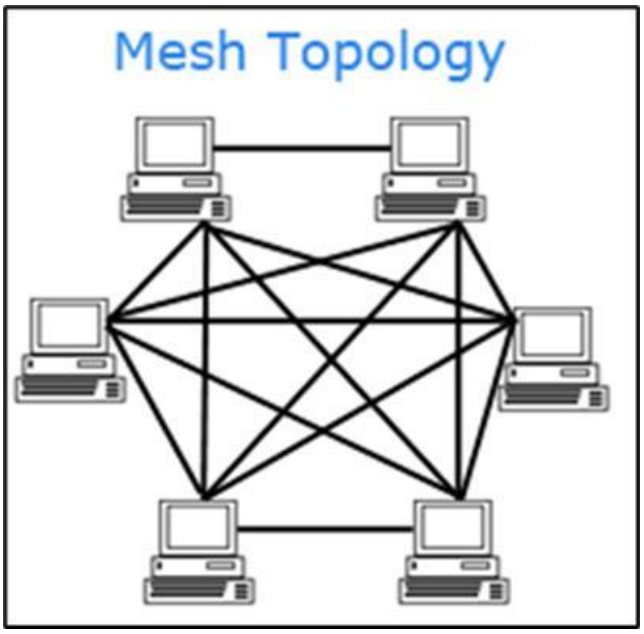

Figure 2.1: MESH topology

2.2.2 BUS topology

From definition, bus topology is a network setup where each computer and network device are connected to a single cable or backbone. Based on Figure 2.2 all data is transferred across the main cable, the maximum distance of the main cable to connect to the devices are limited. Due to this, when error occur in the system it hard to detect where were the faulty and it can be hard to troubleshoot individual device issues. Plus, the findings of the lag innetwork demonstrate that the ring is rather ahead of the bus due to better link load balancing [2]. Despite all of the disadvantages, bus topology is the top list when create asmall system or network and consume less wired connection. So, less cost required whenbuild this network.

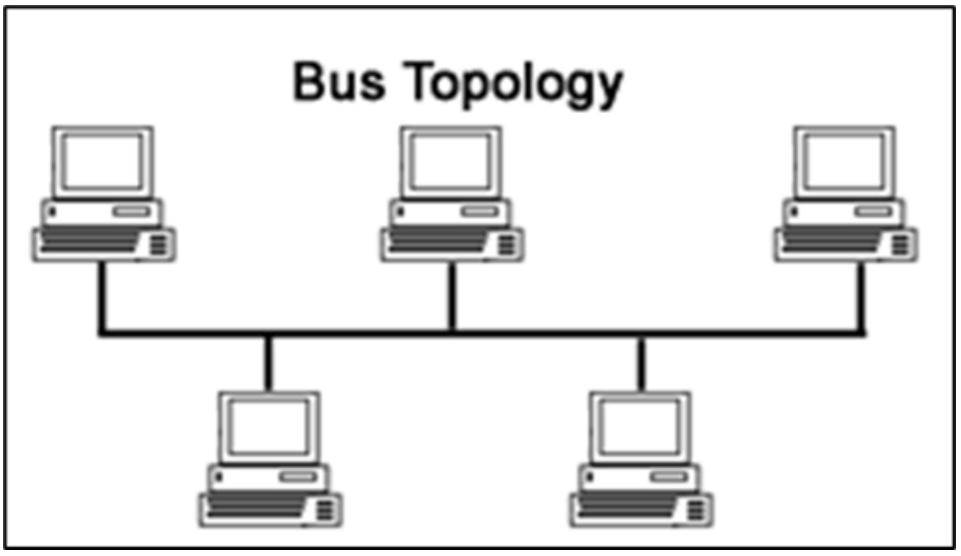

Figure 2.2: BUS Topology

2.2.3 RING topology

For ring topology design in Figure 2.3, a network configuration where device connections create a circular data path. In other word, all connected nodes are interconnected others, like vertices on a circular pattern. When a packet of data is transferred from one unit to the next in the ring network until it finally arrives, this topology is activated. Most ring topologies, known as one-way rings, allow packets to move in just one direction. Other data can transport data across both routes, which is known as two - way data movement. Besides, each device in a ring topology has a repeater, and if the data received is destinedfor another device, the repeater forwards it until it reaches the specific destination. The advantages of using this topology are it is easy to install and to manipulate the number ofdevices that connected. The main issue is if a connection having an error or failure, the whole network will fail due to data been transfer must go through others device to the data reach final destination required by users [3]. This case may cause a network traffic problem in the system.