SOFT ERROR DETECTION IN ADDER SYSTEM

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Bachelor of Engineering

Electrical and Electronics Engineering with Honours

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Grade: _____

Please tick (√)

Final Year Project Report ☐

Masters ☐

PhD ☐

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SOFT ERROR DETECTION IN ADDER SYSTEM

NUR AISYA JASMIN BINTI MAZLAN

A dissertation submitted in partial fulfilment
of the requirement for the degree of
Electrical and Electronics Engineering with Honours

Faculty of Engineering

Universiti Malaysia Sarawak

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To my beloved family and friends

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ABSTRACT

Soft error can be simplified as a disruption that occurred in the circuit. Soft error can cause a malfunction in the whole digital system. The common source of soft error is caused by radiation and due to a charged particle strike at a sensitive node. It also can be called as Single Error Upset (SEU). The reliability of the digital system was disrupted and reduce because of this event. By conducting this project, the error will be detected in different configuration of circuit with the existence of adder system and c-element by using a logic gate. The adder system that will be used for this project is 8-bits Kogge-Stone Adder. Through this project, the configuration of the circuit will be designed, and the results will be compared and analysed one by one in order to get the desired result. An error will be injected into the circuit in order to imitate the soft error event that can occurred in the system. The error will try to be detected later by using logic gates. Each of the results will be analysed and recorded. By using Quartus Altera design software, this project can be conducted properly, and the circuits can be designed as what has been proposed.

ABSTRAK

Ralat lembut boleh dipermudahkan sebagai gangguan yang berlaku dalam litar. Ralat lembut boleh menyebabkan kerosakan pada keseluruhan sistem digital. Sumber biasa ralat lembut disebabkan oleh sinaran dan disebabkan oleh serangan zarah bercas pada nod sensitif. Ia juga boleh dipanggil sebagai Single Error Upset (SEU). Kebolehpercayaan sistem digital telah terganggu dan berkurangan kerana peristiwa ini. Dengan menjalankan projek ini, ralat akan dikesan dalam konfigurasi litar yang berbeza dengan kewujudan sistem penambah dan "c-element" dengan menggunakan get logik. Sistem penambah yang akan digunakan untuk projek ini ialah 8-bit Kogge-Stone Adder. Melalui projek ini, konfigurasi litar akan direka bentuk, dan hasilnya akan dibandingkan dan dianalisis satu persatu bagi mendapatkan hasil yang diinginkan. Ralat akan disuntik ke dalam litar untuk meniru peristiwa ralat lembut yang boleh berlaku dalam sistem. Ralat akan cuba dikesan kemudian dengan menggunakan get logik. Setiap keputusan akan dianalisis dan direkodkan. Dengan menggunakan perisian reka bentuk Quartus Altera, projek ini dapat dijalankan dengan baik, dan litar boleh direka bentuk seperti yang telah dicadangkan.

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LIST OF ABBREVIATIONS

ALU	Arithmetic Logic Design
BPSG	*Borophosphosilicate glass*
BKA	Brent-Kung Adder
CD	Code Detector
C_{out}	Carry Out
C_{in}	Carry In
CMOS	Complementary Metal Oxide Semiconductor
DI	Delay Insensitive
DRAM	Dynamic Random-Access Memory
ECC	Error Correcting Code
EDAC	Error Detection and Correction
FSM	Finite State Machine
GB	Gigabyte
KSA	Kogge-Stone Adder
MB	Megabyte
QDI	Quasi Delay Insensitive
RAM	Random-Access Memory
ROM	Read-Only Memory
s	Sum
SEU	Single Event Upset
SI	Speed Independent
SRAM	Static Random-Access Memory
x	Input data

y	Input data

Chapter 1

INTRODUCTION

1.1 Introduction

For this chapter, there will be a short explanation about the project that will be discussed to give a brief insight and the main idea of this project. Besides, the problem statement and the objectives of this project were also included to clarify the main goal of this project which based on title “Soft Error Detection in Adder System”. The overview of this report was also discussed in this chapter.

1.2 Project Overview and Background

People continue to develop new circuit designs in order to achieve a goal that promotes the advancement of improved design approaches for reducing and decreasing the energy consumption of electronic systems, as well as their faster and wider industrial use. With the increased usage of mobile communication and information terminals, where a compact cell must endure for an extended length of time, low-power design became critical. Furthermore, high-performance electronics suffers from an ongoing increase in the dissipated power per square millimetre of silicon as a result of rising clock speeds, which causes reliability concerns and cooling or restricts performance.

Digital technology is used to store, process, and communicate data. They are employed in a variety of applications, including digital equipment, process control, consumer products, and communication system. The digital computer, commonly known as the computer, is a typical digital system.

The complementary metal-oxide-semiconductor (CMOS) technology is constantly evolving, and nanoscale circuits are becoming increasingly sensitive to soft errors triggered by single event particles as a result of current technological scaling. The current

trend keeps shrinking the device but still having a great performance or even better than the previous device including increasing the operating speeds and reduce the power supply in order to save the energy. These goals are making the device become more complex than before. This indicates that radiation-induced particle impacts from radioactive decay and cosmic rays are becoming increasingly sensitive to digital designs. Soft delays, radiation-induced clock jitter and pulse, and single event (SE) coupling noise and delay effects are a few strategies that have been shown to increase CMOS performance.

The adder system is an important component of the data path. The common prefix adder system in the industry is Brent-Kung adder (BKA) and Kogge-Stone adder (KSA) where it is a common adder design that are preferable to use in processors today.

Soft errors in state holder circuits are a critical concern because they can cause a malfunction to the whole digital system. In asynchronous circuits, C-elements are one of the most common state bearers. If a low-energy particle flips a gate's output and propagates to a circuit output, it causes a soft error. Soft error tolerance has thus become an important requirement in the design of digital systems. The energy efficiency, latency, and area of the three most prominent CMOS implementations of the C-element are compared, with an emphasis on energy. This project is research about soft error detection in adder system.

1.3 Problem Statement

A soft error is a short-term error caused by a particle striking a circuit with enough energy to modify and manipulate the state. SEU occurrences can cause digital circuit faults in a variety of situations, including those sensitive nodes with just enough energy, striking any combinational logic, and impacting control signals such as the clock signals. By conducting this project, some of the problem statement that can be solve are:

1. How to detect soft error in the adder system?
2. What is the effect of soft error towards the adder system?

1.4 Objectives

The objectives of this project are:

1. To compare the effect of soft error at different node in adder system.

2. To determine the existence and absence of soft error in an adder system by analysing the change in the output waveform.

1.5 Project Scope

By considering the problem statement and objectives of this project, the scope of this project is to understand and compare the of different configuration of the circuit with adder system that can help to detect the Single Event Upset (SEU) in the digital system.

1.6 Summary

In this part, the structure of the report was summarized. This report contains several sections including key theories of this project, the previous research related to the project and the theoretical simulations. This report is divided into five chapters which including the introduction, literature review, methodology, research analysis and conclusion. The outline of this report was described as follows:

Chapter 1 represents the overall idea of the project. From this chapter, the main motivation and background of this project will be discussed. The project was introduced including the main objectives and problem statement of the project. The brief explanation of soft error, synchronous design circuit and asynchronous design circuit are mentioned.

Chapter 2 represents the backgrounds and theories which is gathered from various researchers and different perspective that is related to the project. It can be used to support the results after doing the simulation or project. By having all of the information that needed for this project, the project is hopefully can be conducted through the most preferable way.

Chapter 3 represents the suitable method to achieve the objectives of the project. In this part, the breakthrough of flow and development of this project will also be explained