Implementation of Verilog HDL in Calculator Design with FPGA Simulation

Shamsiah binti Suhaili
Department of Electric and Electronic Engineering
Faculty of Engineering
94300 Kota Samarahan, Sarawak
sushamsiah@unimas.my

Kayle Jacqueline anak Kumar
Department of Electric and Electronic Engineering
Faculty of Engineering
94300 Kota Samarahan, Sarawak
kylejac16@gmail.com

Norhuzaimin Julai
Department of Electric and Electronic Engineering
Faculty of Engineering
94300 Kota Samarahan, Sarawak
jnorhuza@unimas.my

Maimun Huja Husin
Department of Electric and Electronic Engineering
Faculty of Engineering
94300 Kota Samarahan, Sarawak
hhmaimun@unimas.my

Mohd Faizrizwan Mohd Sabri
Department of Electric and Electronic Engineering
Faculty of Engineering
94300 Kota Samarahan, Sarawak
msmfaizrizwan@unimas.my

Asrani Lit
Department of Electric and Electronic Engineering
Faculty of Engineering
94300 Kota Samarahan, Sarawak
lasrani@unimas.my

***Abstract*— A calculator is a device that can be found in daily life. This paper proposed the design of a calculator using Verilog HDL. A series of synthesizable Verilog code was created and simulated on Quartus II 15.0. The design of an 8-bit calculator can solve mathematical operations such as addition, subtraction, multiplication, division, square and cube functions, square root and factorial. This calculator consists of eight-digit numbers. In this paper, among the family devices in Altera, Cyclone V was used to perform the simulation process. The outputs are shown in the RTL viewer and waveform simulation of the calculator design. The implementation of a calculator was successfully designed using Verilog HDL in terms of digit numbers and the operation of the calculator function.**

Keywords—Calculator, Verilog, Digital design, Mathematical operation

I. INTRODUCTION

The calculator is an electronic hardware or software device that can carry out simple arithmetic operations such as addition, subtraction, multiplication and division. A scientific calculator has some advanced operations such as trigonometry function, hyperbolic function, exponential function and logarithmic function, which could solve complicated mathematics problems. The invention of calculators has reduced the required time to explain complex figures and common errors when digits are calculated by hand [1, 2].

Scientific calculators support even more transistors in the integrated circuits to carry out the performance of advanced mathematical calculations. The inputs data to the calculators are processed in binary form. The integrated circuit will then convert the decimal numbers into a binary number system, which in the base-two system. Integrated circuits use the binary strings of data to control the transistors for the performance of mathematical calculations. Once the mathematical operations are completed, the binary data will be converted back into the base-ten system. The output will appear on the display screen [3, 4]. Adder is formed by combining several logic gates to get a complex circuit. Different combinations of logic gates in the chips can perform various mathematical calculations like addition, subtraction, multiplication and division.

The digital design developers face challenges to create faster designs with more significant numbers of gates and physically smaller. FPGA designers have to create designs that meet the essential criteria that other designers can understand for performing the chip under worst-case temperature. Besides, the process variation conditions are reliable, testable and can be proven to meet the specification and do not exceed the power consumption goals. Therefore, the designers write hardware description language (HDL) code that will be used for synthesis, and the code will be implemented in the hardware chips. Simulation and operational testing of the outputs using Verilog are vital as they help avoid the error, which may cost much in silicon turns and schedule delays [5 - 13]. The Verilog simulation provides no-cost experiment, and the software tools are cheap of free for testing equipment in FPGA logic [14]. Hardware Description Language such as Verilog HDL and VHDL was used to create systems on chips with schematics. RTL is the design abstraction that controls the modeling of a synchronous digital circuit in the digital signals between hardware registers in the digital circuit design and performs logical operations on the signals. There are lots of research have been done related to calculator design such as calculator design with RISC (64 bit) architecture using Verilog and FPGA, Translation of Division Algorithm into Verilog HDL, A New ALU Architecture Design using Reversible Logic, 12-Bit Verilog Calculator with Trigonometry Functions, Simple 8-Bit Calculator Design Bit Slicing Technique and FPGA Prototyping, Simplified VHDL Coding of Modified Non-Restoring Square Root Calculator, A New Algorithm for Designing Square Root Calculators based on FPGA with Pipeline Technology [15 - 21].

II. OBJECTIVES

This research focuses on the design of a Verilog HDL calculator based on FPGA. The improvement of this calculator can be accomplished by adding the function and the calculator's digit number. The objective of this study is to design eight digits calculator with several different functions using Verilog HDL.

III. DATA TYPE AND FLOW OF THE DESIGN

Figure 1 shows the block diagram of the data type and flow of the calculator design. First, the input values were given to the design, which is in decimal form and converted

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