Analysis of Gate Poly Delayering in SOI Wafer

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***Abstract*—The advantages of silicon-on-insulator (SOI) technology are reduced parasitic device capacitance, improved performance as well as smaller build area. Despite the gains of SOI technology to manufacturers, new challenges arise in Physical Failure Analysis (PFA). The process of delayering polysilicon or active layer becomes impossible without harming the top silicon. This study discussed the challenges of the current fastest, reliable and reproducible method to delayer polysilicon and divulge active layer. Current delayering method using 49% Hydrofluoric (HF) concentration and SC1 solution is proven to be a faster way to reveal polysilicon layer for Bulk Commentary Metal-Oxide Semiconductor (Bulk CMOS). Thus, this method was tested on SOI Wafer to analyze the effect. The experiment was conducted by selecting small, thin and dense gate polysilicon such as in Static Random Access Memory (SRAM) cells. The result shows that high concentration of HF is not suitable for SOI since HF will etch Interlayer Dielectric (ILD) all the way down to Buried Oxide (BOX) and leave top silicon unattached. As a result, top silicon structure was peeled off or damaged. The result was not promising since the top silicon is crucial part as it holds information to discover physical cause of failure.**

***Index Terms*—SOI; Top Silicon; Physical Failure Analysis; Bulk CMOS.**

I. INTRODUCTION

The silicon-on-insulator (SOI) wafer increases chip functionality without the cost of major process equipment changes such as higher resolution lithography process tools. The advantages are faster circuit operation, reduced parasitic device capacitance, smaller devices build area and lower operating voltages [1]–[5]. The lower voltages, low power consumption and high performance for today requirements disclosed the limitations of Bulk Commentary Metal-Oxide Semiconductor (Bulk CMOS) [6].

In SOI wafers, transistors are formed on top of silicon layer which are isolated from the main body of the wafer by an insulator layer, usually silicon dioxide known as Buried Oxide (BOX). Underneath the BOX layer is a support surface wafer which called a 'handle' silicon wafer [5]. Since the SOI technology is differently structured as compared to Bulk CMOS, new challenges in Physical Failure Analysis (PFA) emerge [7]. For instance, challenges in layer de-processing technique or known as delayering method.

Delayering is a process of removing layer on a die to analyst visibility and access to Region of Interest (ROI) at below surface which cannot be accessed or seen. Visibility offers access to Defect of Interest (DOI) for chemical and physical characterization. On the other hand, delayering method also enables electrical accessibility to signal for failure site isolation. Due to increasing interconnect layers and shrinking feature sizes, delayering has become a complex process which requires high skill. Error in delayering can result in a loss of key information which is useful to discover physical cause of the failure.

Some common delayering methods in semiconductor are using dry or wet etching. In dry etching, plasmas or etchant gasses are used to remove material from wafer. This method utilizes high kinetic energy of particle beams, chemical reaction or combination of both to actively remove the material. In wet etching delayering, liquid chemical or etchant is used to etch away material from a wafer. Masks are employed on a wafer for a specific pattern etching. Material surfaces that are not protected by the masks will be etched away by dry or wet etching activity. The masks are deposited and patterned on the wafers in a previous fabrication step using lithography. Material etching activities will remove the material isotropically, anisotropically or both actions at the same time. Isotropic etching is uniform in all direction while anisotropic etching is uniform in vertical direction [8].

Another technology to delayer Integrated Circuit (IC) structures and other microelectronic devices is to use a Chemical and Mechanical Planarization (CMP). CMP uses liquid chemical and spinning pad to improve material removal rates. The CMP is the only process which can delayer and at the same time do planarization on a global scale [9]. Some hard material in a wafer-like tungsten (W) layer is efficiently removed by CMP delayering [10]. In Physical Failure Analysis (PFA), a similar delayering and planarization method is employed which known as parallel lapping.

This work focused on applying the best method in delayering Bulk CMOS into SOI wafer. In this paper, the delayering method and analysis result are discussed. The results of this experiment will hopefully give some brainstorming ideas on how to improve the delayering process for SOI Wafer.

II. METHODOLOGY

Gate poly delayering process in Bulk CMOS is shown in Figure 1. The method can be considered as the fastest way to remove all stacked layers of Intermetallic Dielectric (IMD). Commonly high concentration of Hydrofluoric (HF) acid