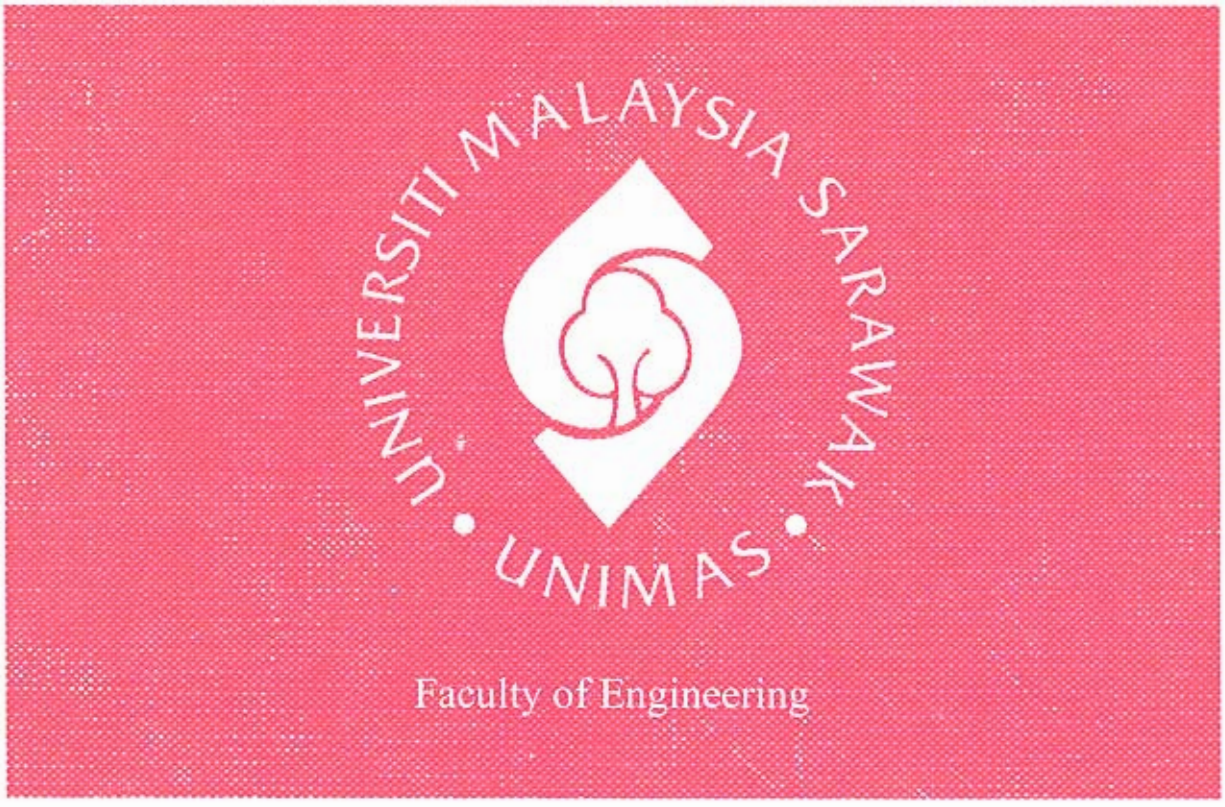


POWER OPTIMIZATION OF LOW NOISE AMPLIFIER

Abdul Haafidz bin Ramli

Bachelor of Engineering (Hons) in
Electronics (Telecommunications)
2014

I declare that Project/Thesis is classified as (Please tick (√)):

☐ **CONFIDENTIAL** (Contains confidential information under the Official Secret Act 1972)*
☐ **RESTRICTED** (Contains restricted information as specified by the organisation where research was done)*
☑ **OPEN ACCESS**

Validation of Project/Thesis

I therefore duly affirmed with free consent and willingness declare that this said Project/Thesis shall be placed officially in the Centre for Academic Information Services with the abiding interest and rights as follows:

- This Project/Thesis is the sole legal property of Universiti Malaysia Sarawak (UNIMAS).
- The Centre for Academic Information Services has the lawful right to make copies for the purpose of academic and research only and not for other purpose.
- The Centre for Academic Information Services has the lawful right to digitalise the content for the Local Content Database.
- The Centre for Academic Information Services has the lawful right to make copies of the Project/Thesis for academic exchange between Higher Learning Institute.
- No dispute or any claim shall arise from the student itself neither third party on this Project/Thesis once it becomes the sole property of UNIMAS.
- This Project/Thesis or any material, data and information related to it shall not be distributed, published or disclosed to any party by the student except with UNIMAS permission.

Student signature _____ (24.07.2014)
(Date)

Supervisor signature: _____
(Date)

Current Address:
14 UNION GARDEN, LORONG STAPOK SELATAN 3, BATU KAWA
93250, KUCHING, SARAWAK

Notes: * If the Project/Thesis is **CONFIDENTIAL** or **RESTRICTED**, please attach together as annexure a letter from the organisation with the period and reasons of confidentiality and restriction.

[The instrument is duly prepared by The Centre for Academic Information Services]

POWER OPTIMIZATION OF LOW NOISE AMPLIFIER

ABDUL HAAFIDZ BIN RAMLI

Thesis is submitted to

Faculty of Engineering, Universiti Malaysia Sarawak

in partial fulfilment of the requirements

for the degree of Bachelor of Engineering (Hons) in

Electronics (Telecommunication)

2013/2014

TO MY BELOVED FAMILY, FRIENDS AND MY LOVE

ACKNOWLEDGEMENT

Alhamdulillah, thanks to Almighty ALLAH S.W.T. for giving me a chance to complete this project. All the good encouragement, devotions, and prayers are due to ALLAH whose blessing and guidance have helped me throughout the entire project.

I would like to thank my project supervisor, Mdm. Dayang Nur Salmi Dharmiza binti Awang Salleh, for her knowledgeable guidance and support which leads to the complete success of this project. I appreciate all the valuable time she spent on the progress of the project on weekly basis until the final completion.

My thanks also go to my beloved family and friends who provide invaluable morale supports and advices, especially during hard times of the project development. I would like to thank them for their caring understanding and patience throughout the project development duration.

ABSTRACT

Low noise amplifiers are widely used in wireless communications. LNA can be found in almost all RF and microwave receivers in both commercial and military applications such as cellular phones, WLANs, Doppler radars and signal interceptors. This paper describes power optimized CMOS low noise amplifier (LNA) intended for Bluetooth application. Employing CMOS inverter as a core of the proposed LNA, the extra gain is obtained by adding a second stage gain control mechanism which is to control the gain. A comprehensive method to optimize CMOS Inverter Current Reused (CICR) family is attained and with gain control mechanism implementation to achieve low noise and high 1dB compression point simultaneously without increasing any circuit and power consumption. The designed LNA is based on 0.18μm CMOS technology and overall performance using simulation environment is presented in this paper.

ABSTRAK

Peguat hingar rendah digunakan secara meluas dalam sector komunikasi tanpa wayar. Ia digunakan dalam hampir semua penerima frekuensi radio dan gelombang mikro samada ketenteraan mahupun komersial. Contohnya, telefon bimbit, WLANs, Radar Doppler dan pemintas isyarat. Kertas kerja ini membentangkan penoptimuman kuasa penguat hingar rendah CMOS yang dispesifikasikan untuk aplikasi Bluetooth. Penyongsang CMOS digunakan sebagai teras kepada penguat hingar rendah yang dicadangkan. Lebih gandaan voltan telah diperolehi dengan menambah peringkat kedua iaitu mekanisma kawalan gandaan voltan yang berfungsi untuk mengawal gandaan voltan. Kaedah yang menyeluruh dilakukan untuk pengoptimuman penyongsangan penggunaan semula arus penguat hingar rendah (CICR) telah dicapai. Pelaksanaan mekanisma kawalan gandaan voltan untuk mencapai hingar rendah dan mampatan 1dB yang tinggi pada masa yang sama tanpa meningkatkan penggunaan kuasa. Reka bentuk penguat hingar rendah ini berpandukan kepada 0.18μm teknologi CMOS dan prestasi keseluruhan dengan menggunakan suasana simulasi dibentangkan dalam kertas kerja ini.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF ABBREVIATIONS

RF	-	Radio Frequency
LNA	-	Low Noise Amplifier
NF	-	Noise Figure
CMOS	-	Complementary Metal Oxide Semiconductor
CG	-	Common Gate
CCCT	-	Capacitive Cross-Coupling Technique
CICR	-	CMOS Inverter Current Reuse
S_{11}	-	Input Return Loss
S_{21}	-	Gain
IIP_3	-	Input Intercept Point

CHAPTER 1

INTRODUCTION

1.1 Introduction to Low Noise Amplifier

Low noise amplifiers are widely used in wireless communications. Almost all RF and microwave receivers in both commercial and military applications such as cellular phones, WLANs, Doppler radars and signal interceptors use LNAs. Depending upon the system in which they are used, LNAs can adopt many design topologies and structures. In commercial applications LNAs aim toward high integration, and low voltage and bias currents. LNAs are usually placed at the front end of a receiver system, immediately following the antenna. The purpose of the LNA is to boost the desired signal power while adding as little noise and distortion as possible [1].

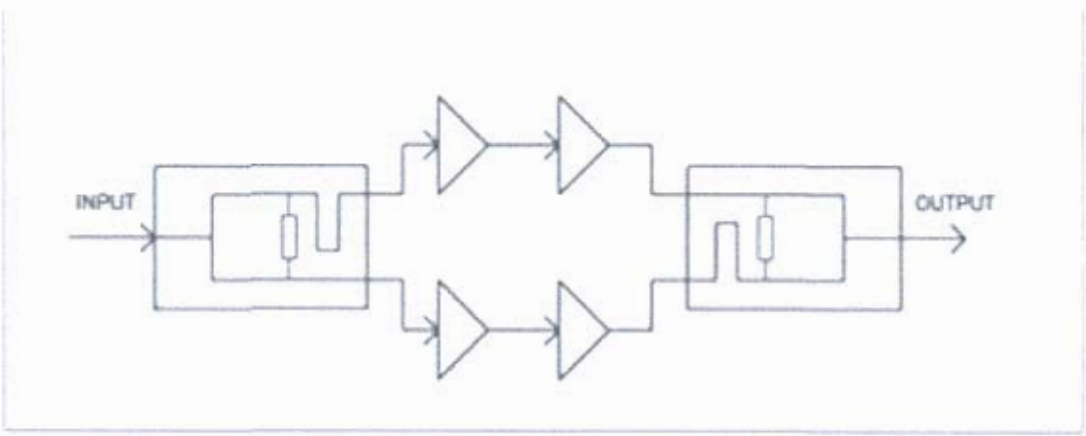


Figure 1.1 Basic topology of LNA [1]

General considerations of LNA design is governed by several parameters. They are noise figure, gain, input return loss, stability, linearity, bandwidth, and power dissipation. It is well known that the first amplification stage dominates the total NF of the system and thus the noise optimization of this first stage is important [2].

1.1.1 *Noise Figure*

The noise figure of the LNA directly adds to that of the receiver. Typical noise figure is at 6 to 8dB, LNA having about 2 to 3 dB, antenna switch of duplexer at 0.5 to 1.5dB and remaining chain about 2.5 to 3.5 dB. While these values provide a good starting point in the receiver design, the exact partitioning of the noise is flexible and depends on the performance of each stage in the chain.

1.1.2 *Gain*

The gain of the LNA must be large enough to minimize the noise contribution of later stages.

1.1.3 *Input Return Loss*

The input return loss can be expressed as the quality of the input match, defined as the reflected power divided by the incident power. Input matching between the antenna/LNA could improve the overall performance. Poor matching at the input cause voltage attenuation, uncharacterized loss, and significant reflections.

1.1.4 *Stability*

In the situation the user of a cell phone wraps his/her finger around the antenna, the antenna impedance changes. For all source impedances at all frequencies, the LNA must remain stable.

1.1.5 *Linearity*

In most application, the LNA does not limit the linearity of the receiver. Thus, LNA design and optimization are done with little concern for the linearity.

1.1.6 *Bandwidth*

The LNA -3 dB bandwidth must be substantially larger than the actual band so that the roll-off at the edges remains below 1dB.

1.1.7 *Power dissipation*

In most receiver designs, circuit's power dissipation is less focused compared to the noise figure.

1.2 CMOS and Power Optimization of Low Noise Amplifier

A proportional downscaling of the supply voltage is required to maintain the device reliability. At the same time, a relatively large threshold voltage (V_t) needs to be maintained to limit the OFF current in transistors, as shown in Figure 1.2 [3].

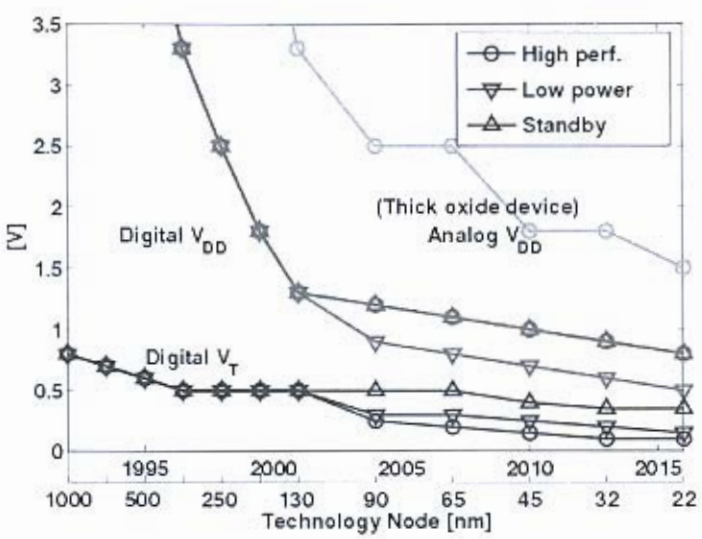


Figure 1.2 Supply and threshold voltage scaling over time as line widths decrease [3]

Portability and reliability are important in low power circuit design. It is due to the use of portable electronic devices mainly laptop and mobile phones. The need for greater portability and reliability affects the limitation on battery weight and size, inducing severe constraint on system power dissipation.

Up until recently, there has been considerable interest in the use of CMOS low-noise amplifiers (LNA) for RF and wireless systems, especially frequency modulation (FM) radio receivers. Such a radio receiver can be used as an expansion of a variety of portable audio devices such that the devices can offer FM radio reception. For RF integrated Circuits (RFIC) operating at FM frequency bands (centered around 100 MHz), an on-chip inductor is rarely used for the LNAs [4].

Driven by the insatiable demands for lower costs and higher bandwidth, technology is moving towards higher integration while operating at lower supply voltages. As process geometries decrease, operating voltages must be scaled down due to the increased electric fields and reduced breakdown voltages caused by higher doping profiles. This decrease is suitable for low power consumption devices. However, the threshold voltage (V_{th}) of a MOS transistor decreases at a much lower rate than the supply voltage with the decreasing CMOS process. This limitation makes the RFICs design more difficult, hence new topologies are needed to face the complexity due to the lowered supply voltage and improve the overall performances [5].

From the figure below, it is observed that scaled down device yields wider range of threshold voltage (V_{th}).

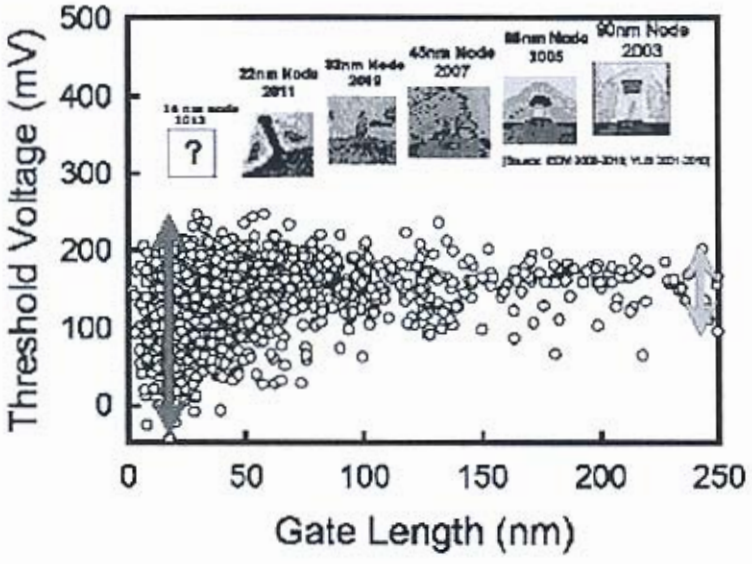


Figure 1.3 Gate length and voltage threshold trends [6]

Furthermore, low-cost and compactness, low power consumption, high linearity in the pass band, and acceptable stability increase its practical importance. In order to enhance the quality of front end amplifiers' operation, they should be considered as a whole rather than a single block; i.e., all the elements included in the structure must be studied, designed, and optimized simultaneously. Techniques are developed to optimize power in LNAs. Among The published optimization techniques are mostly applied to either common source (CS) or cascade LNAs [7].

Typical applications of 2.4GHz, such as Bluetooth, promise mass market development with high volume production. Wireless control and communication between a mobile phone and a headset, or another Bluetooth component is few of the applications of available in the market.

1.3 Objectives

The objectives determined for this project are as shown below:

- Develop and implement design techniques to achieve power optimization of LNA
- Design CMOS LNA for Bluetooth application

1.4 Report Outline

Chapter 1 is an introduction to the project including the basic of low noise amplifier, the significance of power optimization, and objectives and overall development.

Chapter 2 provides an overview research associated to the project. Reviews based on the power optimization are conducted and theories are reviewed. Related techniques are reviewed and understanding on the most preferred technique is determined. Comparisons on different technique are conducted.

Chapter 3 describes the methodology developed by chosen techniques used to design the LNA. Two stage design of the LNA is developed. Each design is studied carefully to achieve the specification performance of the LNA. Procedures for obtaining the overall performance are added by using the Virtuoso Analog Environment simulation.

Chapter 4 contains the simulation results acquired from the techniques used to design the LNA. Detail analyses are discussed based on the simulation output reading under the Virtuoso Analog Environment simulation.

Chapter 5 is the conclusion of the report. Recommendations are presented in this chapter for resolving the constraints encountered during the project.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, comparisons of low noise amplifier (LNA) topologies are conducted to identify the technique used for power optimization application. It is suggested from the preliminary studies that the gain, noise figure and input matching is the main concern in LNA design. These topologies, which are common gate (CG), CMOS inverter current reused (CICR), single stage cascade, and digital gain control are techniques that have been used for power optimization application.

2.2 Differential Common Gate (CG) Active Boost Low Noise Amplifier (LNA)

In 2011, Francois Belmas, Frederic Hameau, Jean-Michel Fournier proposed an inductorless low power (LP) low noise amplifier (LNA) based on the common gate (CG) topology. Gain boosting techniques is combined to enable high gain LP LNA.

The proposed circuit composed of a "main" amplifier (NMOS M_{1A-B}, R1) and a so-called "g_m-boost" amplifier (NMOS M_{3A-B}, R3). There are 3 reasons for the use of CG topology. First, CG circuits are known to be more linear [8]. Secondly, auxiliary CG circuits helps in lowering the input impedance. Thirdly, with C_{C2} when cross coupling technique (CCCT) is applied, it boosts the g_m-boost amplifier without extra P_{DC}. R_3 is defined as the output load of the gm-boost amplifier and by using

current sources M_{5A-B}, excessive voltage drop is avoided. The gain bandwidth is enhanced with neutralization capacitors (C_{C4}) that cancel the gate-to-drain capacitance of M_1 and creates a peaking effect on the g_m-boost gain.

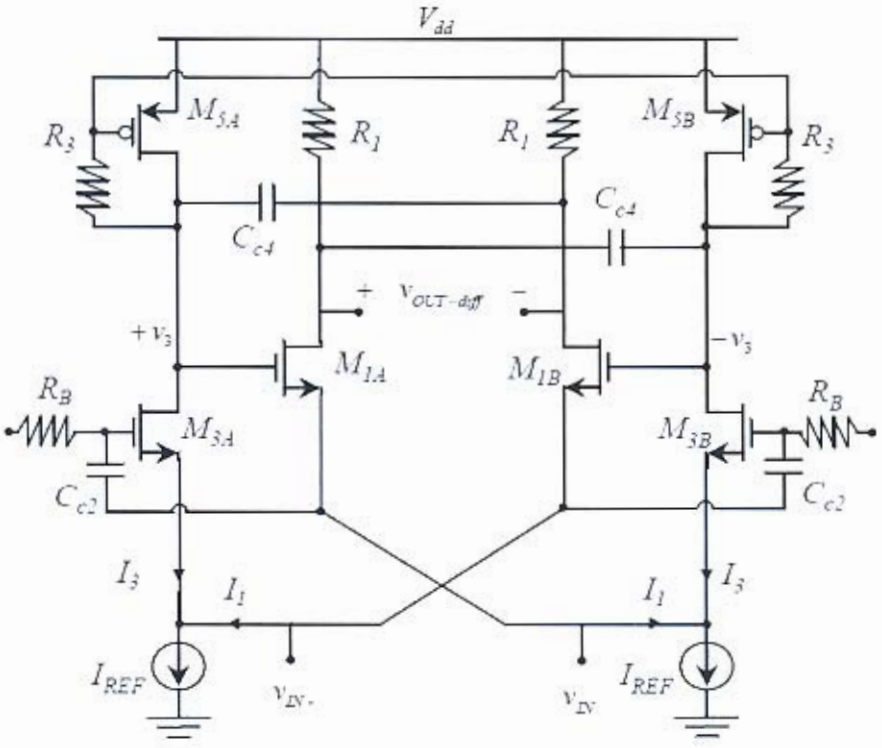


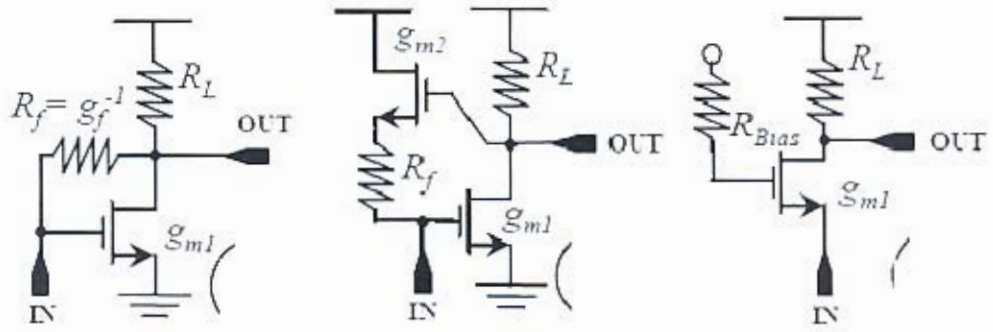
Figure 2.1 Schematic of differential CG active boost LNA [9]

2.2.1 Input matching technique and gain boost

In most applications, most inductorless LNA circuits with the input 50Ω impedance are either based of shunt-feedback (SFB) structure or common gate (CG) topology [10]. It is noted that high voltage gain, good input matching with low power consumption are required. SFB is built with a pure resistive feedback, where input admittance G_{IN} is the ratio of the voltage gain A_V and resistive feedback R_F.

For Figure 2.2(a), R_F does of consume power but degrades the output impedance and, thus, the gain capability when g_{m1} is small. Alternatively, using a source follower along with R_F is conducted in Figure 2.2(b) but the extra P_{DC} required for g_{m2} limits the performance of the amplifier. Lastly, using common gate

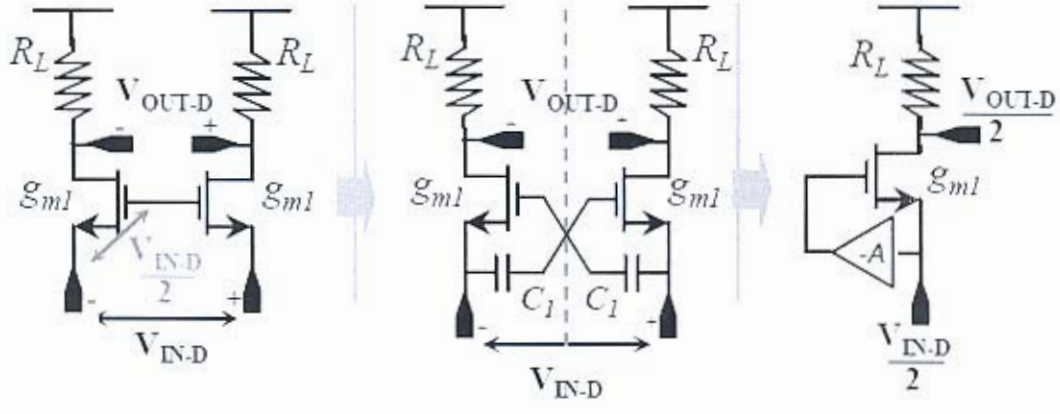
(CG) circuits as in Figure 2.2(c) enable both higher gain and lower input impedance when g_{m1} increases but the condition of input matching forces g_{m1} to be equal to 1/50Ω=20mS thus making it not suitable for input matching at low P_{DC}.



(a) (b) (c)

Figure 2.2 Comparison of (a) Resistive SFB, (b) Active SFB, (c) Common Gate

Figure 2.3 illustrate g_m enhancement technique that is applied to increase the gain. The P_{DC}-g_m tradeoff in common gate (CG) amplifier is avoided. Applying a cross coupling techniques (CCCT), the AC amplifier current is doubled. This technique is known as gate voltage booster by enabling a g_m-boost effect since the equivalent g_m is doubled for constant biasing current [11].



(a) (b) (c)

Figure 2.3 Techniques (a) Differential CG amplifier, (b) Differential CG amplifier with CCCT, (c) Principle of g_m-boost in CG amplifier

2.2.2 Design Parameter

2.2.2.1 *Input Matching and Gain*

The equivalent voltage gain (G_V) and input admittance (G_{IN}) are:

$$G_V = g_{m1}R_1(1 + 2g_{m1}R_3) \qquad (2.1)$$

$$G_{IN} = g_{m1}(1 + 2g_{m1}R_1) + 2g_{m1} \qquad (2.2)$$

These values are affected by the loading conditions of the LNA. The 50fF load capacitor strongly affects the final bandwidth. R_1 and R_3 need to be high to provide high gain and low noise and 2.45GHz gain cut-off frequency is acquired. Hence, C_{C4} is chosen to make the LNA stable. As shown in the Figure 2.4, high capacitance value does not affect the bandwidth but increase the high frequency gain roll-off.

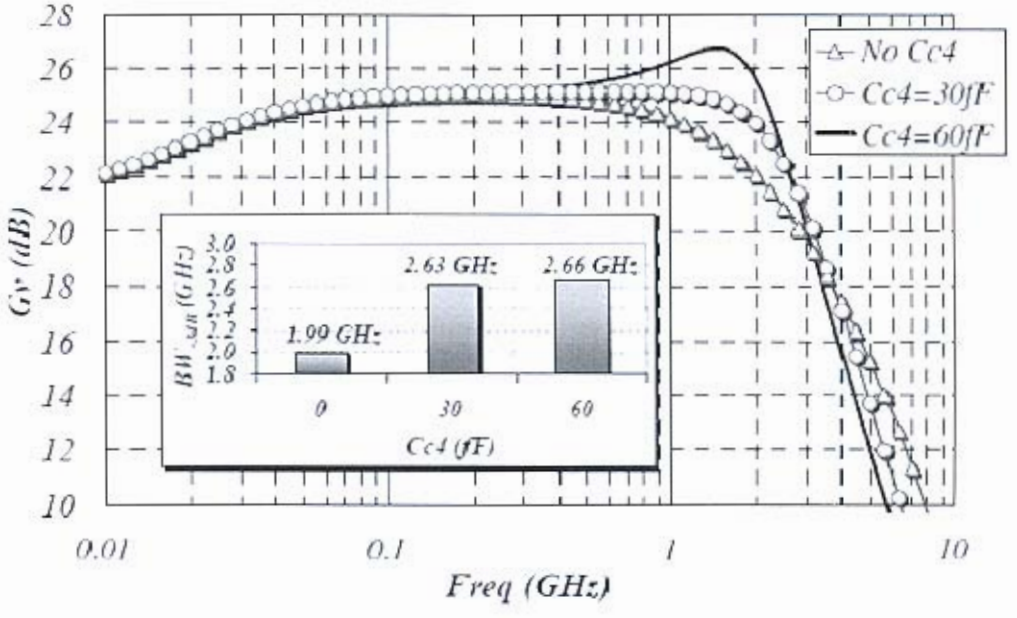


Figure 2.4 Effect of neutralizing capacitor C_{C4} on gain bandwidth and IIP_3 [9]

2.2.2.2 *Noise Performance*

g_m-boost amplifier is made of active noisy components. Designing at low bias current, extra noise sources have to be included. From Figure 2.5, the unmatched

noise factor of full CGAB LNA is calculated. The main reason of using CCCT on g_m-boost is to reduce the noise contributors by half, without the P_{DC} penalty.

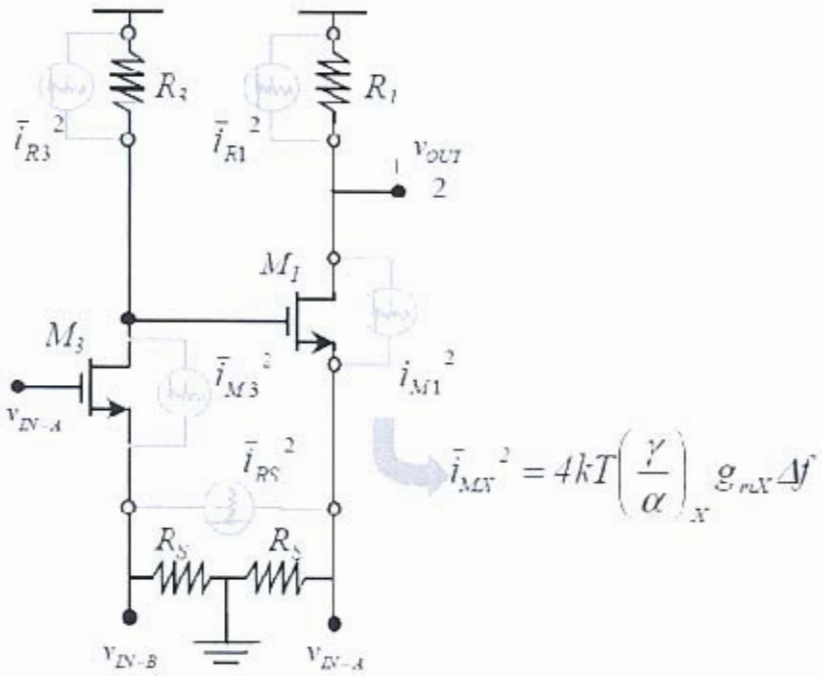


Figure 2.5 Equivalent circuits for noise calculation (2.3 and 2.4) [9]

$$F = 1 + F_{M3} + F_{R3} + F_{M1} + F_{R1} \tag{2.3}$$

$$F \approx 1 + \frac{(\frac{\gamma}{\alpha})_3}{2g_{m3}R_S} + \frac{1}{2g_{m3}^2R_3R_S} + \frac{2(\frac{\gamma}{\alpha})_1}{g_{m1}R_S(1+A_3)^2} + \frac{2(1+g_{m3}R_S+g_{m1}R_S(\frac{A_3}{2}))^2}{g_{m1}^2R_1R_S(1+A_3)^2} \tag{2.4}$$

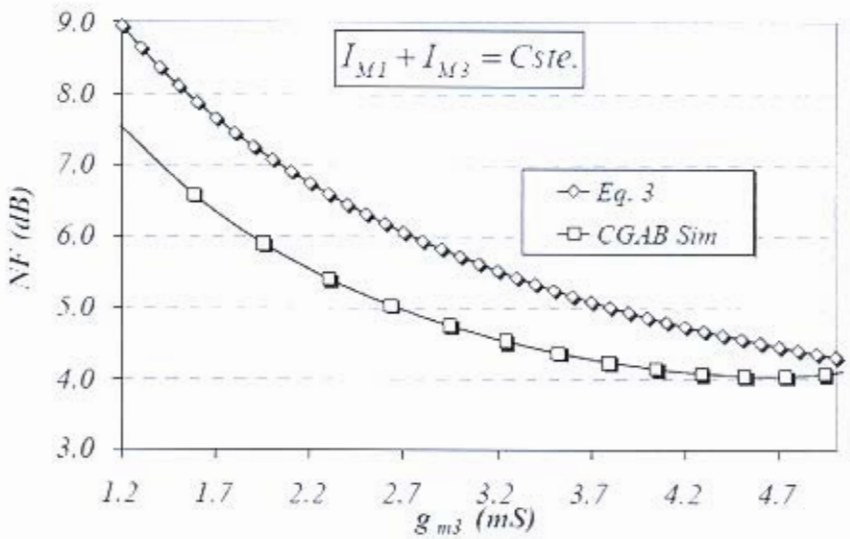


Figure 2.6 Simulated and calculated NF vs g_{m3}, as I_{M1} decreases, I_{M3} increases [9]