



Faculty of Engineering

THE DESIGN OF OPTIMUM INVERTER

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**Bachelor of Engineering with Honors
(Electronics & Telecommunications Engineering)
2010**

UNIVERSITI MALAYSIA SARAWAK

R13a

BORANG PENGESAHAN STATUS TESIS

Judul: THE DESIGN OF OPTIMUM INVERTER

SESI PENGAJIAN: 2009/2010

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THE DESIGN OF OPTIMUM INVERTER

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Thesis is submitted to

Faculty of Engineering, Universiti Malaysia Sarawak

in partial fulfilment of the requirements

for the degree of Bachelor of Engineering

with Honours (Electronic and Computer Engineering) 2010

Dedicated to my beloved family and friends

ACKNOWLEDGEMENTS

This project has been made possible as a result of the co-operation and support rendered by several individuals. While it is impossible to list down all of them, I am very grateful for their assistance.

Firstly, I would like to extend a very special note of appreciation to my supportive Final Year Project supervisor, Madam Nurdiani who has put so much effort in coordinating this project. I am thankful to her patience, advices, comments and guidance throughout the course of this project. Her patience and guidance throughout this project is greatly appreciated.

I also would like to thank to all lecturers in Electronics Department who have offered their advice. Their advice and help was especially helpful in improving my writing and knowledge. Grateful gratitude also dedicated to anyone who directly or indirectly helps in making this project success.

Lastly, I would like to thank my family and friends for all their love, care, support and companion that had helped me go through the many hard days in lives and studies all these while. Thank you.

ABSTRACT

This report presents the design and analysis of the inverter. The design is based on the CMOS inverter that consists of PMOS and NMOS transistors. The analysis is based on the current leakage and time delay during switching the inputs to be output. Up to 20 different transistor sizes were implemented in the same design with varying transistor width, W and length, L . The optimum size of W and L of the transistor will improve the current leakage and time delay of the CMOS inverter. The CMOS is designed using computer simulation and analysis is done using the MICROWIND simulation system. This report also provides a basic understanding of chips design and how performance of simulation can be done. The information will help to design the optimum inverter.

ABSTRAK

Kajian ini bertujuan untuk merekabentuk dan menganalisa penyesuai isyarat. Rekabentuk tersebut menggunakan penyesuai isyarat CMOS yang mengandungi transistor PMOS dan NMOS. Analisa pula berdasarkan arus yang keluar dan sela masa yang digunakan semasa operasi penukaran isyarat masuk kepada isyarat keluar. Hampir 20 jenis saiz transistor digunakan dalam rekaan yang sama dengan berlainan lebar, L dan panjang, P. Saiz yang optima dapat mengurangkan kadar arus yang keluar dan sela masa dalam penyesuai isyarat CMOS. CMOS direka dengan simulasi komputer dan dianalisa menggunakan simulasi dalam MICROWIND. Kajian juga memperkenalkan pengetahuan asas untuk merekabentuk chip dan meningkatkan prestasi rekaan dalam simulasi.

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ABBREVIATION

t_r	-	Rise time
t_f	-	Fall time
t_p	-	Propagation delay
C_L	-	Load capacitor
V_{DD}	-	Source voltage
V_{in}	-	Input voltage
V_{out}	-	Output voltage
GND	-	Ground
R_{ON}	-	On-resistance
V_{GS}	-	Voltage gate-to-source
V_T	-	Threshold voltage
t	-	Time
CLK	-	Clock timing
V_m	-	Mid voltage
IC	-	Integrated circuit
θ_{jA}	-	Thermal resistance
μm	-	Micrometer

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The inverter is the most basic gate of all digital design. It transforms the output logic into opposite of the input logic. For example, in binary code the input is '1' then the output is '0' and vice versa if the input is '0' then the output is '1'. In others example, if the input is 'ON' then the output is 'OFF' and vice versa when the input is 'OFF' and the inverter gate is applied the output is 'ON'.

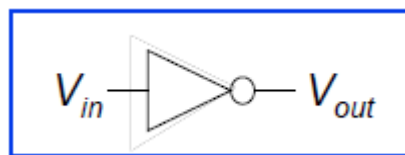


Figure 1.0: The basic diagram of inverter

1.2 Project Overview

The study is about to reduce the current leakage for the inverter if both PMOS and NMOS gates are turned ON. This can be performed by designing the W/L ratio for PMOS and NMOS. Designing the ratio of W/L is to equalize the rise time, t_r and fall time, t_f for the PMOS with NMOS and having the less delay. The value of W/L must be in the range of practical applications. The project is using software MICROWIND to design and simulate the very large scale integration of electronics circuit. In the MICROWIND, the program runs and directly shows the delay between the t_r and t_f .

1.3 Problem of Statement

Inverter has static and dynamic behavior which make it unique gate and can be applied to all integrated circuit. In the ideal condition, the inverter gate should have infinite gain in the transition region and have the input and output impedance of from infinity to zero. Besides that, it must have full rail-to-rail swing in the high noise margin. There also no static current with a low power consumptions [1].

However, in the real world the leakage current is the major problem in designing the inverter. There always leakage current during switching between inputs to output, where there will the static power dissipation occur when both PMOS and NMOS are turn 'ON'. The static power dissipation is the condition where there are direct path between power source and the ground of the inverter.

As the leakage current increased, the delay in the inverter also increased. These problems can be solved by designing the width and length ratio of the inverter which is W/L parameter. But again, the problem is how to choose the optimum size of W/L in order to optimize the inverter performance in term of delay and current leakage.

1.4 Objectives

The main objective of the study is to measure the current leakage in the inverter. Besides that, is to find the ratio of width and length (W/L) of the inverter which consist PMOS and NMOS that has the less delay.

1.5 Scope of study

In this research, the scope of study is to measure the current leakage in the inverter. In order to measure the current leakage in the inverter, the W/L ratio of the PMOS and NMOS must be designed variably at the range of practical used until the optimum value of inverter determined. The value of W/L is related to the propagation delay, t_p of the gate. When optimizing the inverter, meaning is to optimize the t_p of the PMOS and NMOS. Then the delay values can be used to measure and determine the current leakage of the inverter. The software involved to design and simulate the W/L ratio is using MICROWIND. From the MICROWIND, the delay can be analyzed and the value of W/L can be customized.

1.6 Chapters Outline

This report is divided into five main chapters; Introduction, Literature Review, Methodology, Result and Discussion, Conclusion and Recommendations. The summary of the content for each chapter is as following.

Chapter 1 Introduction is the global introduction about inverter. It explains the overview and objectives of the study. It also includes the scopes of study.

Chapter 2 Literature Review contains the background of the study. This chapter covers a number of fundamental properties of digital gates. These parameters help to quantify the performance and reliability of a gate for inverter structure static complementary CMOS. This chapter also covers about the tools and software that involved for analyzing the inverter.

Chapter 3 Methodology is about the approaches that been used in the research. This cover the method and step that needed and also software that been used to do the analysis and design the project. It also states the outline of procedure on how to carry out the study.

Chapter 4 Result and Discussion contain the result of which design is selected and experimental data gained to evaluate the performance of the inverter.

Chapter 5 is the final chapter, which is the Conclusion & Recommendations. The conclusion is based on the objective of the project. The recommendations for future advancements and studies of the project will be will be concluded in this final chapter.

CHAPTER 2

LITERATURE REVIEW

2.1 MOS Transistor Characteristics

NMOS transistor heavily doped n-type source and drain regions are implanted or diffused into a lightly doped p-type substrate. The polycrystalline silicon (polysilicon) is grown over the region between the source and drain. It then forms the gate of the transistor. Neighboring devices are insulated from each other with field oxide or gate oxide and a reverse biased np-diode, formed by adding an extra p^+ region called the channel-stop implant. In NMOS transistor, current is carried by electrons moving through an n-type channel between the source and drain. Figure 2.1 show the cross section of a typical MOS transistor which is typically n-channel.

In addition, there are also current carried by both holes and electrons in pn-diode. It is called PMOS transistor, heavily doped p-type source and drain and having n-type to be the substrate. The current are carried by the holes mobility through the p-channel. In CMOS technology, both NMOS and PMOS are present. NMOS and PMOS devices are fabricated in separate isolated regions called well that are connected to different power supplies.

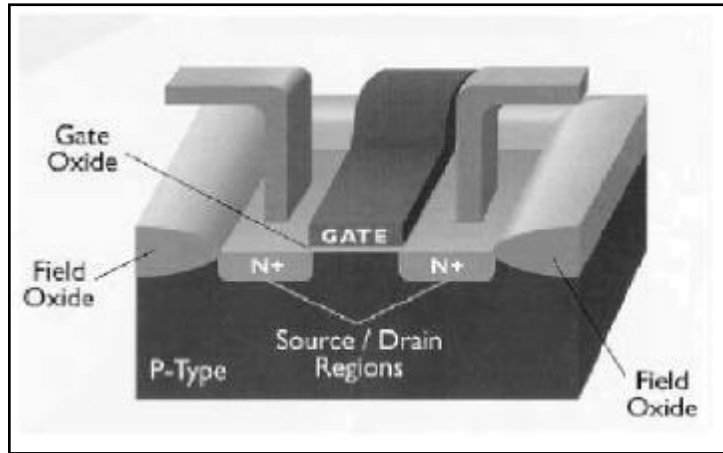


Figure 2.1: MOS transistor [1]
(source from Digital Integrated Circuits © Prentice Hall 1995)

2.2 CMOS Inverter

In ideal CMOS, there is always a path to V_{DD} or ground (GND) in steady state but no direct path between power and GND meaning that no static power dissipation. CMOS have extremely high input resistance and nearly zero input current at the steady state with low output impedance. In CMOS, propagation delay acts as a load capacitance and resistance of the transistors.

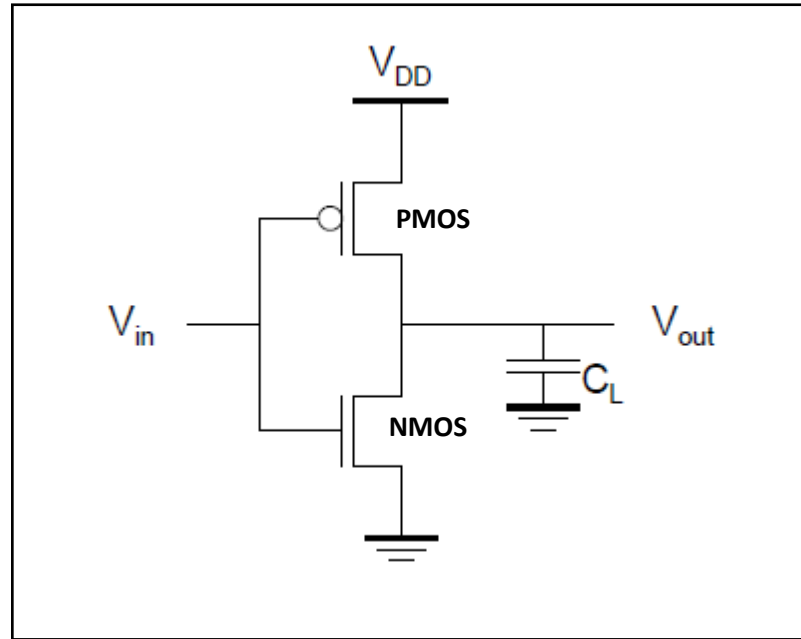


Figure 2.2: Static CMOS inverter. V_{DD} stand for supply voltage

In Figure 2.2, it shows the static CMOS inverter in the circuit level. Qualitatively, CMOS can be modeled as a switch with a finite on- resistance R_{on} . When $|V_{GS}| < |V_T|$, the switch is open and when $V_{GS} > V_T$ the transistor behave as a finite resistance [1]. When V_{in} is high or equal to V_{DD} the NMOS transistor is on while PMOS is off. A direct path exists between V_{out} and GND node resulting in a steady-state value of 0V. In other hand, when the input voltage is low or less than threshold voltage (V_T), then NMOS is off and PMOS is on. There is path between V_{DD} and V_{out} therefore it will yield a high output voltage. Between power supply and GND in steady-state operation there are no path exists and no consume any static power dissipation [1]. The Figure 2.3 shows the switch model in steady state response and the gate behavior.

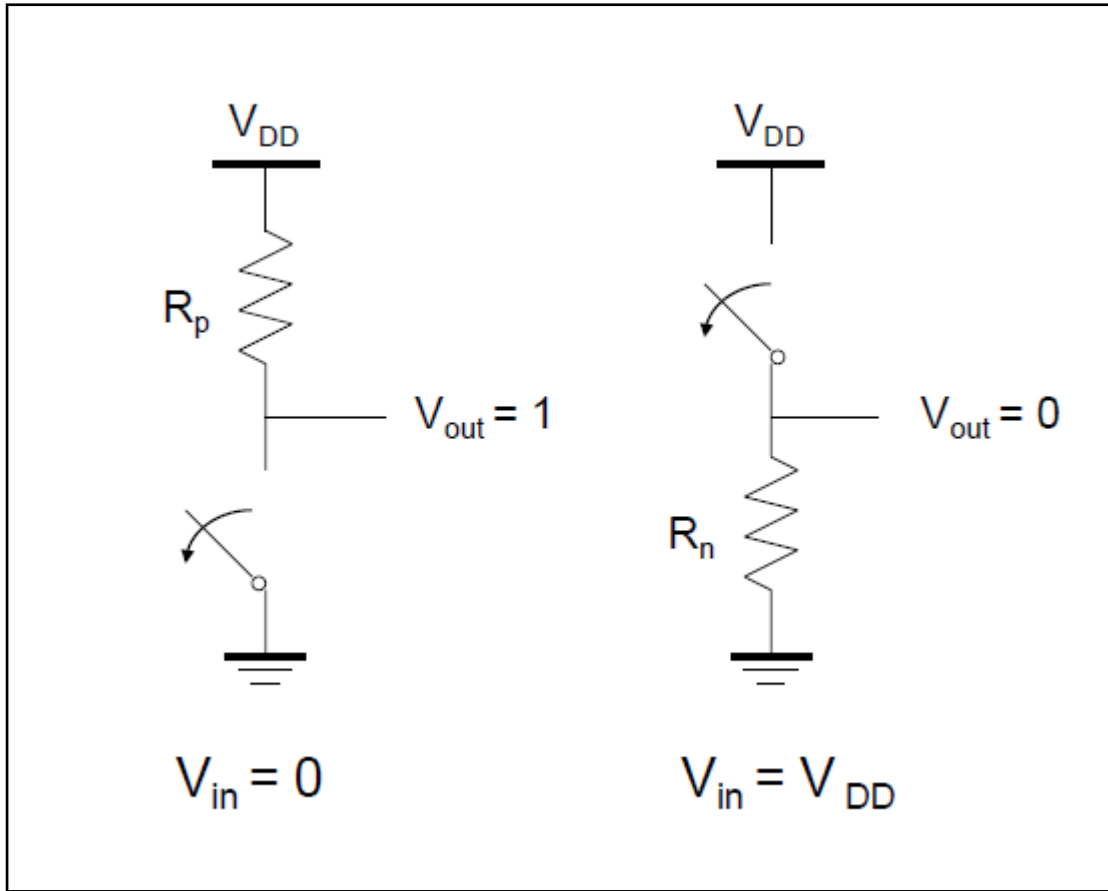


Figure 2.3: Switch model in steady state response

The gate response time is determined by the time to charge C_L through R_p and discharge through R_n . When designing static CMOS circuits, the PMOS section is wider than the NMOS section to balance the driving strengths of the transistors. It is to maximize the noise margins and obtain symmetrical characteristics.

2.3 Static CMOS Inverter

Static CMOS is except during switching where the output connected to either V_{DD} or GND via a low resistance path. From a static perspective, it is an important model because it gives a metric and can be judge from quality of actual implementation [2]. The ideal inverter model has the infinite gain in the transition region and gate threshold located in the middle of the logic swing with high and low noise margin equal to half the swing. Besides that, the input and output impedance of the gate are infinity and zero respectively.

The Figure 2.4 shows the CMOS inverter consists of two devices a pull-up and pull-down. Pull-up is typically either a bipolar junction transistor or an enhancement mode field effect transistor [1]. Pull-down might be another transistor or resistor, current source or diode. PMOS transistor only, pull-up make a connection from V_{DD} to V_{out} and NMOS transistor only the pull-down make a connection from V_{out} to the GND.