PHASE LOCKED LOOP

DAYANG DUWININGSIH BINTI ABANG ABDULLAH

FAKULTI KEJURUTERAAN
Universiti Malaysia Sarawak
2001

Borang Penyerahan Tesis
Universiti Malaysia Sarawak

R13a

BORANG PENYERAHAN TESIS

Judul : **PHASE LOCKED LOOP (IN COMMUNICATION SYSTEM)**

SESI PENGAJIAN : 1998/2001

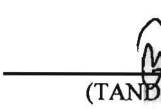
Saya **DAYANG DUWININGSIH BINTI ABANG ABDULLAH**
(HURUF BESAR)

mengaku membenarkan tesis ini disimpan di Pusat Khidmat Maklumat Akademik, Universiti Malaysia Sarawak dengan syarat-syarat kegunaan seperti berikut:

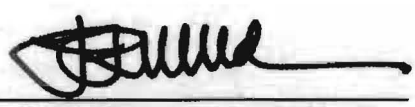
1. Hakmilik kertas projek adalah di bawah nama penulis melainkan penulisan sebagai projek bersama dan dibiayai oleh UNIMAS, hakmiliknya adalah kepunyaan UNIMAS.
2. Naskhah salinan di dalam bentuk kertas atau mikro hanya boleh dibuat dengan kebenaran bertulis daripada penulis.
3. Pusat Khidmat Maklumat Akademik, UNIMAS dibenarkan membuat salinan untuk pengajian mereka.
4. Kertas projek hanya boleh diterbitkan dengan kebenaran penulis. Bayaran royalti adalah mengikut kadar yang dipersetujui kelak.
5. * Saya membenarkan/tidak membenarkan Perpustakaan membuat salinan kertas projek ini sebagai bahan pertukaran di antara institusi pengajian tinggi.
6. ** Sila tandakan (/)

[ ]	SULIT	(Mengandungi meklumat yang berdarjah keselamatan atau kepentingan Malaysia seperti yang temaktub di dalam AKTA RAHSIA RASMI 1972.
[ ]	TERHAD	(Mengandungi maklumat TERHAD yang telah yang ditentukan oleh organisasi/ badan di mana penyelidikan dijalankan).
[/]	TIDAK TERHAD	

Disahkan oleh



(TANDATANGAN PENULIS)



(TANDATANGAN PENYELIA)

Alamat tetap: Lot 1716, Blok B,
Kampung Haji Baki, 93250 Kuching,
Sarawak

Prof. Madya Dr. Mohamad Kadim Hj Suaidi
Nama Penyelia

Tarikh: 17-Apr-01

Tarikh: 26/4/01

CATATAN * **Potong yang tidak berkenaan**
**

Jika Kertas Projek ini SULIT atau TERHAD, sila lampirkan surat daripada pihak berkuasa/ organisasi berkenaan dengan menyertakan sekalitempoh kertas projek. Ini perlu dikelaskan sebagai SULIT atau TERHAD.

This project report entitled "**PHASE LOCKED LOOP**" was prepared and submitted by **DAYANG DUWININGSIH BINTI ABANG ABDULLAH** as a partial fulfillment of the requirement for the Degree of Bachelor of Engineering with honours in Electronic and Telecommunications is hereby read and approved by:

26/4/01

.....

Prof. Madya Dr. Mohamad Kadim Hj. Suaidi
(Supervisor)

.....

Date

PHASE LOCKED LOOP

DAYANG DUWININGSIH BINTI ABANG ABDULLAH

Tesis Dikemukakan Kepada
Fakulti Kejuruteraan, Universiti Malaysia Sarawak
Sebagai Memenuhi Sebahagian daripada Syarat
Penganugerahan Sarjana Muda Kejuruteraan
Dengan Kepujian (Kejuruteraan Elektronik Dan Telekomunikasi)
2001

Dedicated to my beloved parents, Vic , Mash, Karti and Zhafiran

ACKNOWLEDGMENT

First of all, I would like to express my special thanks to my supervisor, Prof. Madya Dr. Mohamad Kadim Suaidi for his guidance and tolerance throughout the process of completing this thesis project.

I wish to express my appreciation to Encik Al Khalid Othman, Puan Sakena Abdul Jabar and Encik Kismet Hong Ping for all of the comments, critiques and suggestions in finalizing my thesis.

I also would like to record my gratitude to all my friends and others with whom I have had conversations that expanded the ideas for this project. who helped me in many ways in this project.

Finally, to my beloved family, especially my parents with thanks for all the years of caring, love and support.

ABSTRACT

Phase locked loop (PLL) is a feedback device which are often found in communication systems. Generally, the transmission of signals in communication system is performed through a transmitter and receiver. PLL is an electronic circuit that consists of phase detector, low pass filter and voltage controlled oscillator. The characteristic in PLL has made it as a preferable method to built the frequency modulator and frequency demodulator. This can be done by doing the simulation process by using MATLAB software.

ABSTRAK

Gelung Terkunci Fasa (PLL) merupakan litar suap balik yang biasanya digunakan di dalam sistem komunikasi. Umumnya, penghantaran isyarat dalam system komunikasi disampaikan melalui alat pemancar dan alat penerima. Gelung terkunci fasa (PLL) adalah litar elektronik yang mengandungi pengesan fasa , penapis laluan rendah dan pengayun terkawal voltan. Ciri-ciri yang terdapat pada "PLL" telah menjadikan ia satu kaedah yang paling sesuai untuk membentuk rangkaian nyahmodulat frequensi dan modulasi frekuensi. Ini boleh dilakukan melalui proses simulasi dengan menggunakan perisian MATLAB.

TABLE OF CONTENTS

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 General background

The basic phase-locked loop (PLL) concept has been known and widely utilized since first being proposed in 1922. Since that time, phase-locked loops have been used in instrumentation, space telemetry and many other applications requiring a high degree of noise immunity and narrow bandwidth [10].

Originated in 1932, phase-locked loop was given a new life by integrated circuit technology. Prior to its availability in a single integrated circuit (IC) package in 1970, its complexity in discrete circuitry form made it economically unfeasible for most applications [1]. System that has been designed using the latest PLL technology has many benefits such as the operation is straight forward and easy to learn , the appliances are compact, light weight and unobtrusive when worn. Apart from that it is low cost and can provide high performance.

Thus, for all these years, phase-locked loops (PLLs) have found wide application in many general purpose such as in control systems, navigation systems, radar, telemetry tracking and especially in communication systems. All this application employ various forms of phase-locked loops to improve performance and enhance capability [10].

1.2 Communication system

Communication system involves the transfer of information from one place to another over relatively long distance [1]. It can be classified as either analog or digital. Some categories of communications systems are radio, television, telephony, radar, navigation, satellite, data and telemetry. Generally, a simple communication system contains three parts, namely, the transmitter, the transmission medium and the receiver. The communication system may use amplitude modulation (AM), frequency modulation (FM) or other modulation techniques to send information. Any method can be used as long as the demodulation method match the modulation process method to recover the transmitted signal correctly. For this thesis project, the modulation and demodulation block in a communication system are concerned. This project focuses on how phase-locked loop can be used with one type of analog modulation, that is frequency modulation (FM), in typical application such as modulator and demodulator.

1.3 Objectives

The main objective of this project is to comprehend essentially how the phase locked loop (PLL) operates. The background and characteristics of PLL and its application will be examined. Meanwhile, the second approach in this project is to learn how the PLL can be applied with FM. Later, the acquired knowledge will be utilized to construct a simulation block diagram of FM modulator and demodulator. MATLAB software will be used for the simulation purpose.

1.4 Thesis Outline

The material in this thesis is organized as following:

Chapter 2 provides a brief literature review on phase locked loop (PLL). Here, the PLL is defined, and basic applications are discussed. The discussion is based on basic concept of PLL such as PLL components, how it operates and its typical specifications. Chapter 3 presents a basic introduction to frequency modulation (FM) and discuss the role of PLL in frequency modulator and frequency demodulator. In this section, FM is defined and how the PLL can be used as frequency modulator and frequency demodulator is reviewed. It also contains all the equations of PLL, FM modulator and FM demodulator. Simulation using MATLAB software is done by using these equations. Chapter 4 describes the MATLAB software. In this section, a short introduction on MATLAB software and the toolbox used for the simulation purpose will be presented. Chapter 5 deals with the simulations, results and discussion. Finally, the conclusion of the project is covered in Chapter 6 with the recommendation in future.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

Phase-locked loop (PLL) is one of the integrated circuits containing both linear and digital circuits. The PLL consists of three basic functional blocks [10]:

1. A phase detector (PD)
2. A low-pass filter (LPF)
3. A voltage-controlled oscillator (VCO).

2.2 Basic concept of PLL

The phase-locked loop is used to track output signal with input signal in frequency as well as in phase and recover it from noise [13]. Figure 2.2-1 illustrate the basic phase-locked loop system. More precisely, a PLL is a circuit synchronizing an output signal generated by an oscillator with the frequency of input signal. In synchronized state, any change in input signal will appears as a change in phase between oscillator signal and input signal. This phase shift acts as an error signal to make the output signal same as the input signal. The locking onto a phase relationship between input signal and the output signal accounts for the name of phase-locked loop.

The idea of the combination of these three parts is to make the PLL an electronic servo capable of locking onto an input-signal frequency so that its output frequency is the same as that of the input reference. A significant criteria of PLL is that the output can be large, clean signal, frequency-locked to a low-level, noisy input signal.

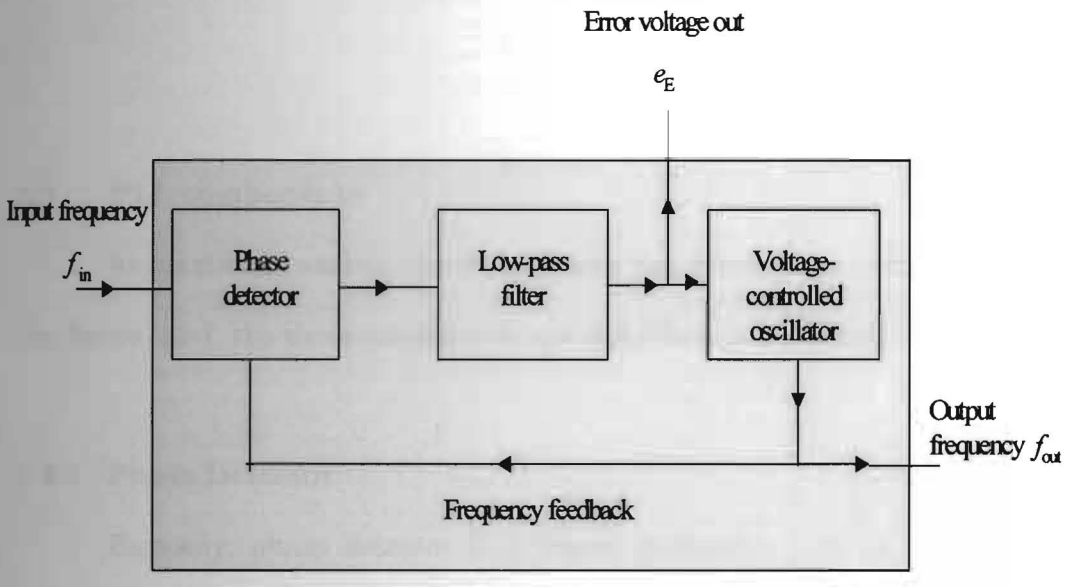


Figure 2.2-1: Basic phase-locked loop system [4]

Figure 2.2-2 shows the simplified representation of phase locked loop. There are three signals in the PLL, one input and two outputs [4]. An input terminal is the input signal to be processed. The output signals are the error signal, e_E and output frequency , f_{out} . The error signal output e_E is proportional to the phase difference between input frequency and output frequency meanwhile the frequency output functions to follow the input signal frequency.

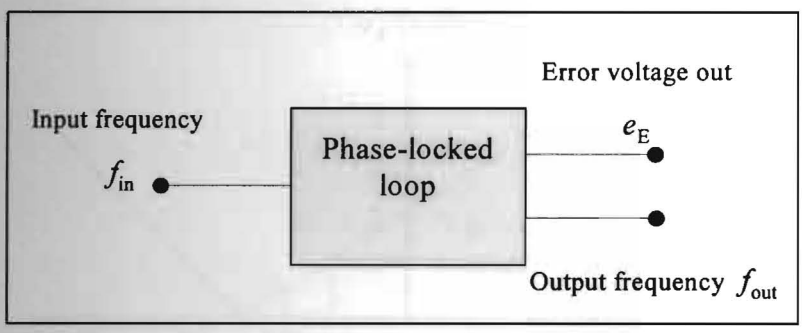


Figure 2.2-2: Simplified representation of PLL [4]

2.3 PLL components

As mentioned earlier, the PLL system has three main parts. Referring to the figure 2.2-1, the three components are describes as following.

2.3.1 Phase Detector

Basically, phase detector is a linear multiplier [11]. It has two input signals, an input frequency f_{in} as the reference signal and output frequency, f_{out} from VCO. The phase detector is perhaps the most important part of PLL system since it is here the input and VCO frequencies are simultaneously compared with each other.

2.3.1.1 Phase Detector Characteristic

The phase difference between the input phase and VCO phase is represented by θ_d. In response to θ_d, a voltage v_d is produced. A free running voltage, V_{do} will be generated when no signal v_i is applied to the phase detector. The phase error is defined as

$$\theta_e = \theta_d - \theta_{do} \qquad (2.3.1.1\text{-}1)$$

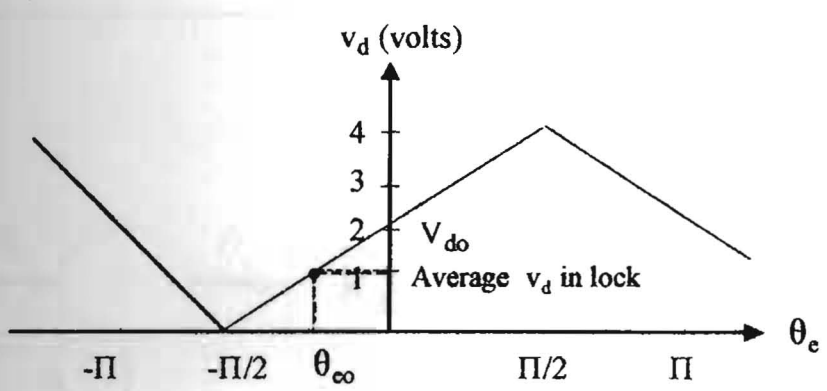


Figure 2.3.1.1-1 : Phase Detector characteristic [5]

Figure 2.3.1.1-1 shows the PD characteristic where v_d versus θ_e. By definition, $v_d = V_{do}$ in response to $\theta_e = 0$. There is a constant slope K_d in the range $-\pi/2 \leq \theta_e \leq \pi/2$. The signal flow graph in fig 2.3.1.1-2 represents the PD model in linear region. It is modeled by

$$v_d = K_d \theta_e + V_{do} \qquad (2.3.1.1\text{-}2)$$

where K_d is the PD gain

θ_e is phase error of the VCO output relative to the input reference.

V_{do} is the free running voltage.

The values of θ_e for which the linear model is valid are the range of phase detector.

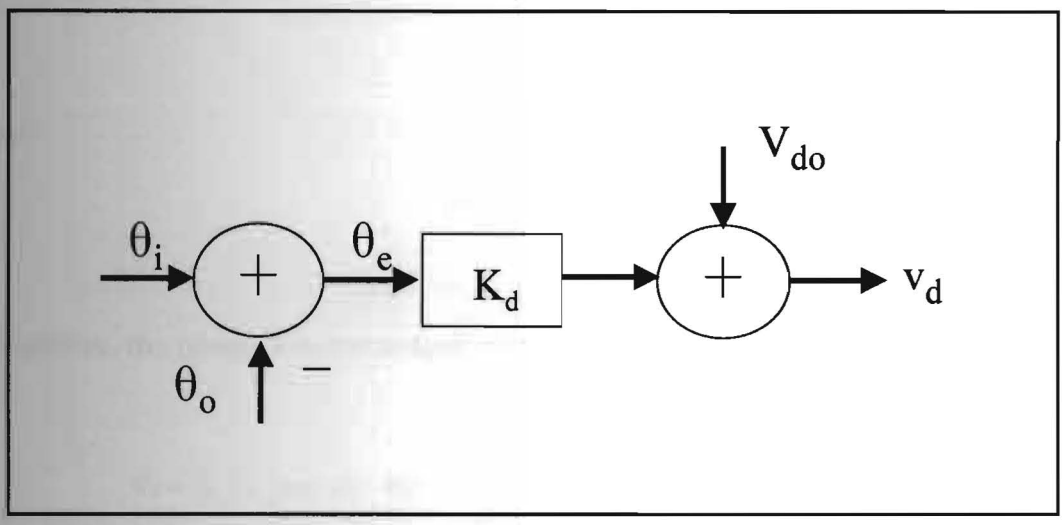


Figure 2.3.1.1-2 : Phase detector model [5]

2.3.1.2 Operation of Phase detector

The expression of input signal, V_i and the reference signal from the VCO, V_o applied to phase detector can be expressed as [11];

$$v_i = V_i \sin (2 \pi f_i t + \theta_i)$$

$$v_o = V_0 \sin (2 \pi f_0 t + \theta_0)$$

where θ_i and θ_0 are the relative phase angles of the two signals.

The phase detector multiplies these two signals and produces a sum and difference frequency output, V_d, as follows.

$$V_d = V_i \sin (2\pi f_i t + \theta_i) \times V_o \sin (2\pi f_0 t + \theta_0)$$

$$= \frac{V_i V_o}{2} \cos [(2\pi f_i t + \theta_i) - (2\pi f_0 t + \theta_0)] - \frac{V_i V_o}{2} \cos [(2\pi f_i t + \theta_i) - (2\pi f_0 t + \theta_0)] \quad (2.3.1.2\text{-}1)$$

When the PLL is in lock,

$$f_i = f_0$$

and

$$2\pi f_i t = 2\pi f_0 t$$

Therefore, the phase detector output voltage is

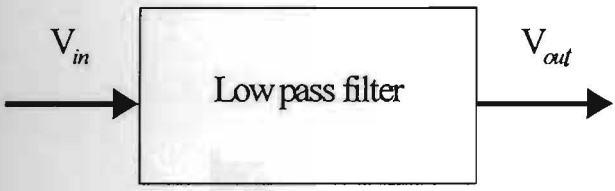
$$V_d = \frac{V_i V_o}{2} [\cos(\theta_i - \theta_0) - \cos(4\pi f_i t + \theta_i + \theta_0)] \qquad (2.3.1.2\text{-}2)$$

2.3.2 Low pass filter

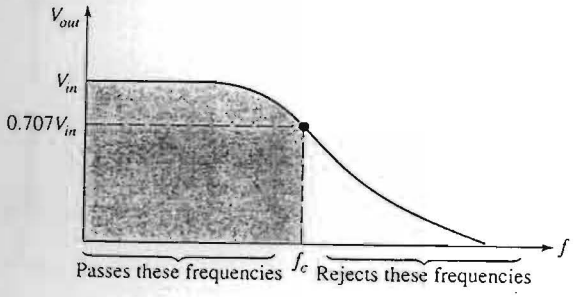
Low- pass filter is a circuit that allows the passage of low frequencies and dc while suppressing high frequencies components of the multiplication of the phase detector [4]. The low- pass loop filter can be passive or active and it can be of any order (first, second, third, etc.) [13]. However, most applications are of the second order. The output of the filter is a dc voltage corresponding to the phase difference of the two inputs at phase detector. This dc voltage is the control voltage for voltage-controlled oscillator.

2.3.2.1 Low - pass filter Characteristic

Low- pass filter acts as an attenuator at high frequencies and have unity gain at dc. In response to this, the bandwidth can be set as desired. The range of frequencies passed by a low pass filter within the specified limit is illustrated in figure 2.3.2.1-1. From the figure, the filter's output voltage is 70.7% of the maximum. This is where the frequency is said critical.



(a)



(b)

Figure 2.3.2.1-1: (a) Low- pass filter model and (b) general response curve

2.3.2.2 Operation of LPF

The second harmonic term ($2 \times 2\pi f_i t$) in Equation 2.3.1.2-2 is filtered out by the low-pass filter. The filter output voltage is expressed as

$$v_c = \frac{ViVo}{2} \cos \theta_e \qquad (2.3.2.2\text{-}1)$$

where $\theta_e = \theta_i - \theta_0$. θ_e is called the phase error. The filter output voltage is proportional to the phase difference between the incoming signal and the VCO signal and is used as the control voltage for the VCO. This operation is illustrated in Figure 2.3.2.2.