High Gain of 3.1-5.1 GHz CMOS Power Amplifier for Direct Sequence Ultra-Wideband Application

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***Abstract*—This paper presents the design a power amplifier (PA) for direct sequence ultra-wideband applications using 0.13 µm CMOS technology operating in a low band frequency of 3.1 GHz to 5.1 GHz. Current-reused technique is employed at the first stage to increase the gain at the upper end of the desired band. Cascaded common source configuration with shunt peaking inductor at the second stage helps to enhance the wideband frequency while increasing the gain approximately twice the performance. The simulation results specify that high gain of 20.3 dB with ± 0.8 dB flatness, group delay variation of ±121.3 ps, and good input return loss and output return loss is obtained over desired working band. The proposed PA achieves power consumption of 27.3 mW.**

***Index Terms*—Power Amplifier; Ultra-Wideband; CMOS; Techniques; Performance Criteria.**

I. INTRODUCTION

In recent year, many researchers involved in new technology i.e., ultra-wideband (UWB) system because of its capability to provide high data rate over short distance range as well as very low power consumption. Two UWB standards have been proposed by IEEE 802.15.3a, namely multiband orthogonal frequency division multiplexing (MB-OFDM) and direct-sequence code division multiple access (DS-CDMA) [1]. BPSK and bi-orthogonal keying (BOK) mode is used for DS-UWB to supports the data communication [2]-[3]. Figure 1 shows DS-UWB signal transmission with two important bands which are low band from 3.1-4.85 GHz and high band from 6.2-9.7 GHz. The advantages of DS-UWB are low cost, high efficiency that will lead to longer battery life, high data rate, robust and accurate spatial resolution for detecting the location.

Various CMOS PA designs for UWB application have been proposed with different techniques such as distributed amplifier [4]–[5], resistive shunt feedback [6]–[9], RLC matching [10], shunt-shunt feedback [11]–[12], shunt peaking [13], inductive source degeneration [14]–[15], current reuse [16]–[17], and stagger tuning [18]–[19]. Each of the technique offers different performance depending with PA specification design.

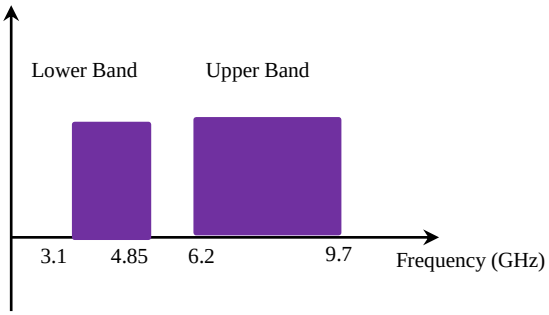

Figure 1: DS-UWB spectrum allocation

The distributed amplifier is commonly used for wide frequency range and can achieve good linearity. However, this technique consumes high power consumption and large chip area compared to other techniques due to the transmission line configuration used in this technique [4]–[5].

The RLC matching is the technique that needs a few reactive components to build RLC filter to provide good matching at the input and output for wideband application. The disadvantage of this technique is it produce large chip area because of a few reactive components is used for filter design [10].

Resistive shunt feedback is amongst popular technique that can offer very wideband matching at the input and output of the circuit [11]–[12]. This technique offers smaller chip area compared to other techniques since it is utilized no inductor or less inductors [20]. Current reuse is one of the topology which can provide low group delay and low power consumption. However, it is difficult to meet the requirement of high gain [16]–[17]. Another fabricated PA reported using stagger technique have shown that very wide band from 3.1 to 10.6 GHz, low group delay, high gain, good gain flatness and small chip area was implemented and designed in PA for UWB application [16]. However, this design consumes very high power consumption up to 100 mW and it is not suitable for UWB application.

In this paper, high gain of 3.1 GHz to 5.1 GHz UWB CMOS power amplifier by adopting current reuse technique is designed using 0.13 µm CMOS technology.